Improved Accuracy and Runtime of IC Power Supply Noise Simulations through Multi-Phase and Voltage Controlled Resistor Analyses

2011 MICRON SENIOR CLINIC
UNIVERSITY OF UTAH

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Presentation Overview

- Project Motivation/Background
  - Importance to Micro-Electronics
- Project Description
  - Multi-Phase Analysis
  - Voltage Controlled Resistor (VCR) Substitution
- My Contribution
  - Tool Flow and Process Design

Micro-Electronics

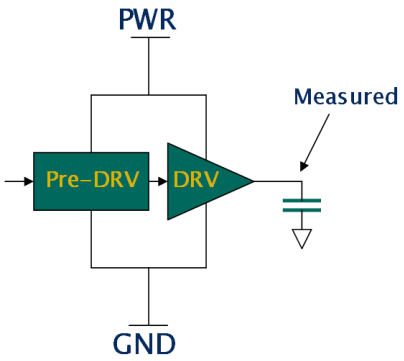
- Consumer Electronics Market is Growing
  - Persistent demand for more gadgets
  - More demand for performance
  - More new technology required

[2]

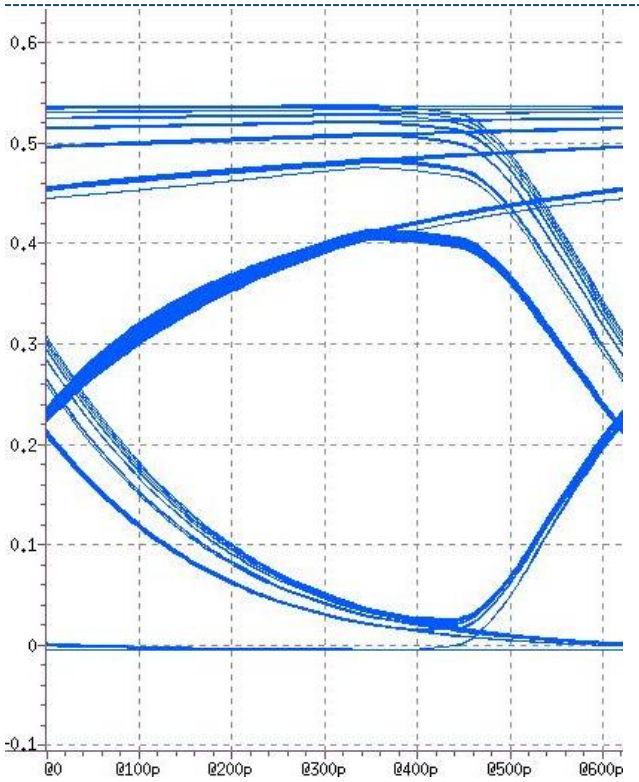
[1]

Modern ICs Getting More Complex

Ideal case:



[6]

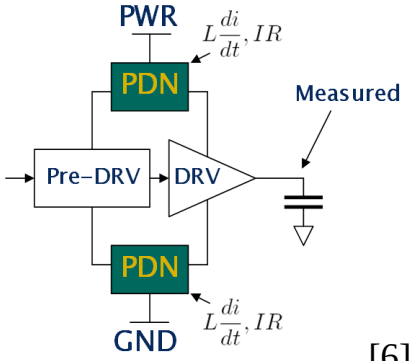


Added Complexities:

- More Transistors
- Higher Frequencies
- Smaller Features
- Lower Power

Non-Ideal = Decreased Circuit Performance

- Non-Ideal Power Supply
  - Parasitic effects
  - Ringing
  - Noise
- Circuit Responds Negatively
  - Effects timing
  - Effects speed



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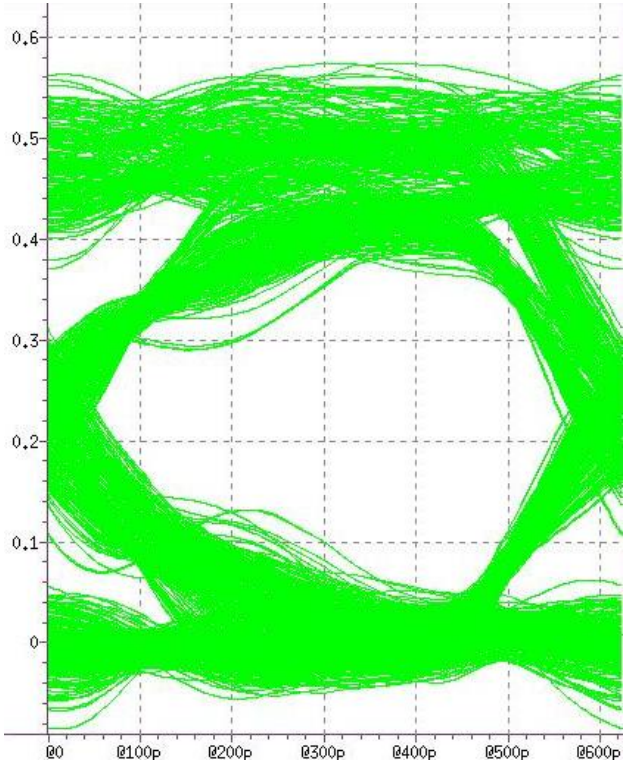
Reality:



Circuit Complexity Challenges

- Requirement for SPICE Simulation
  - Circuit size and complexity make behavior predictions impossible
  - SPICE simulations can give insight as to circuit function

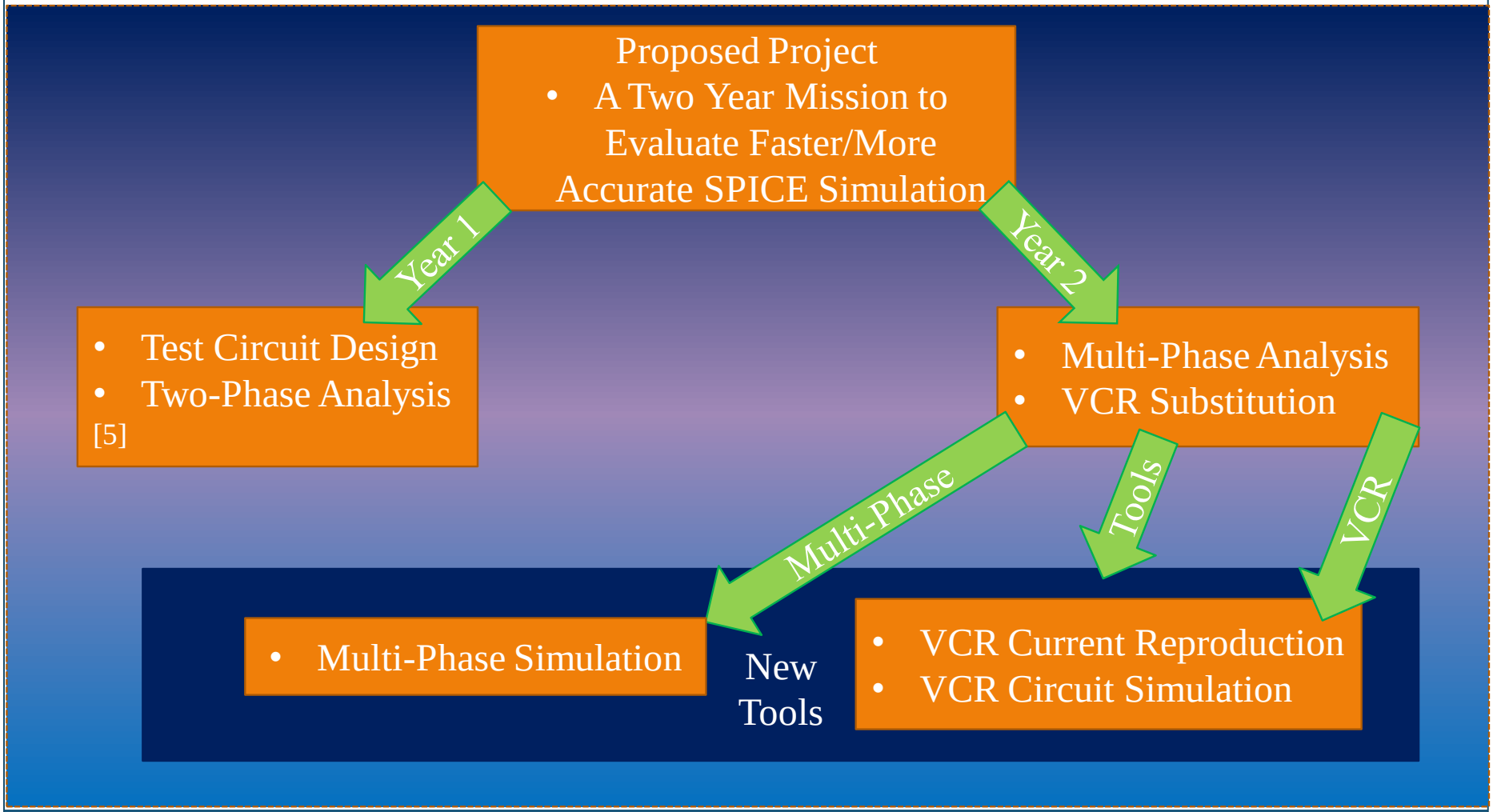
- Industry "Gold Standard"[4] Insufficient
  - Large/complex Hspice simulations unmanageable
  - New simulation strategies must be employed

Attempts to Rectify the Problem

- Industrial Attempts
  - HSIM^{plus} (Synopsis), Voltage Storm (Cadence), Totem (Apache) [3]
  - All Sacrifice Some Accuracy for Speed/Lower Memory Demand

- Current Project
  - Testing Simulation Methods for Viability
  - Open Loop Methodology – Multi-Phase Analysis
  - VCR Substitution Methodology

Project Proposal

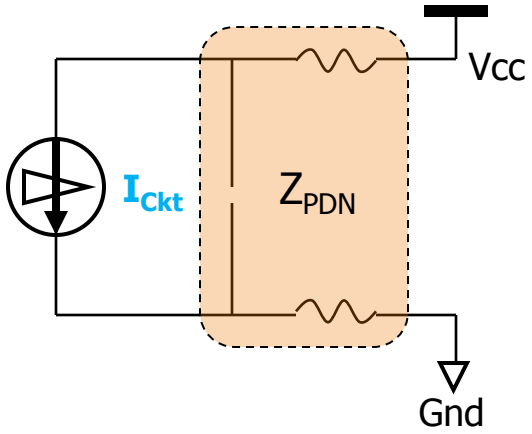


A Description of Two-Phase Analysis

Phase 1:
Run time-domain simulation with all circuitry in place and capture circuit-specific currents into and out of the supplies

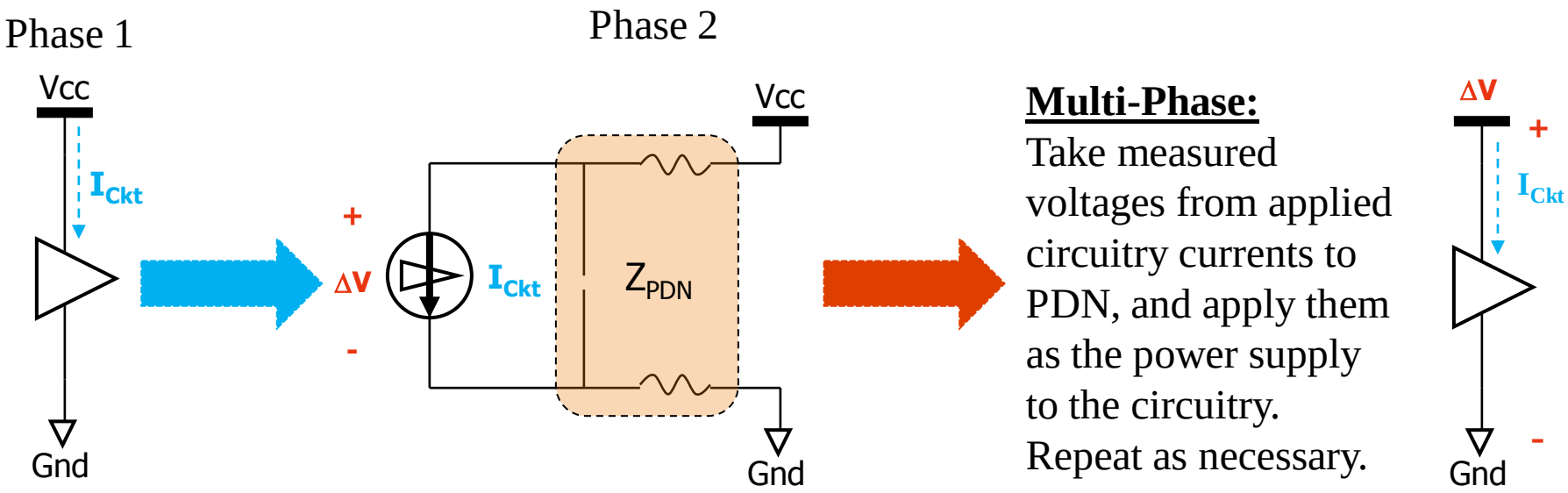
Phase 2:
Apply extracted currents to full Power Delivery Network and capture static and dynamic voltage changes

[3]



Multi-Phase Description

- Multi-Phase Analysis
  - Extension of two-phase strategy to an open loop

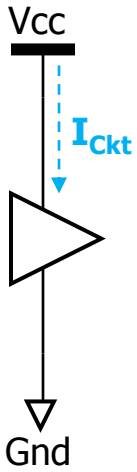


[3]

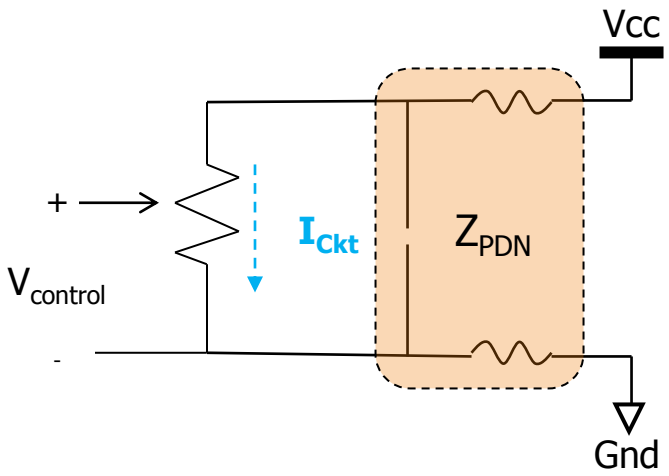
Voltage Controlled Resistor

- Similar to Two-Phase As Well
  - Rather than replace circuitry with current source, replace it with VCR

Phase 1 – Collect Currents

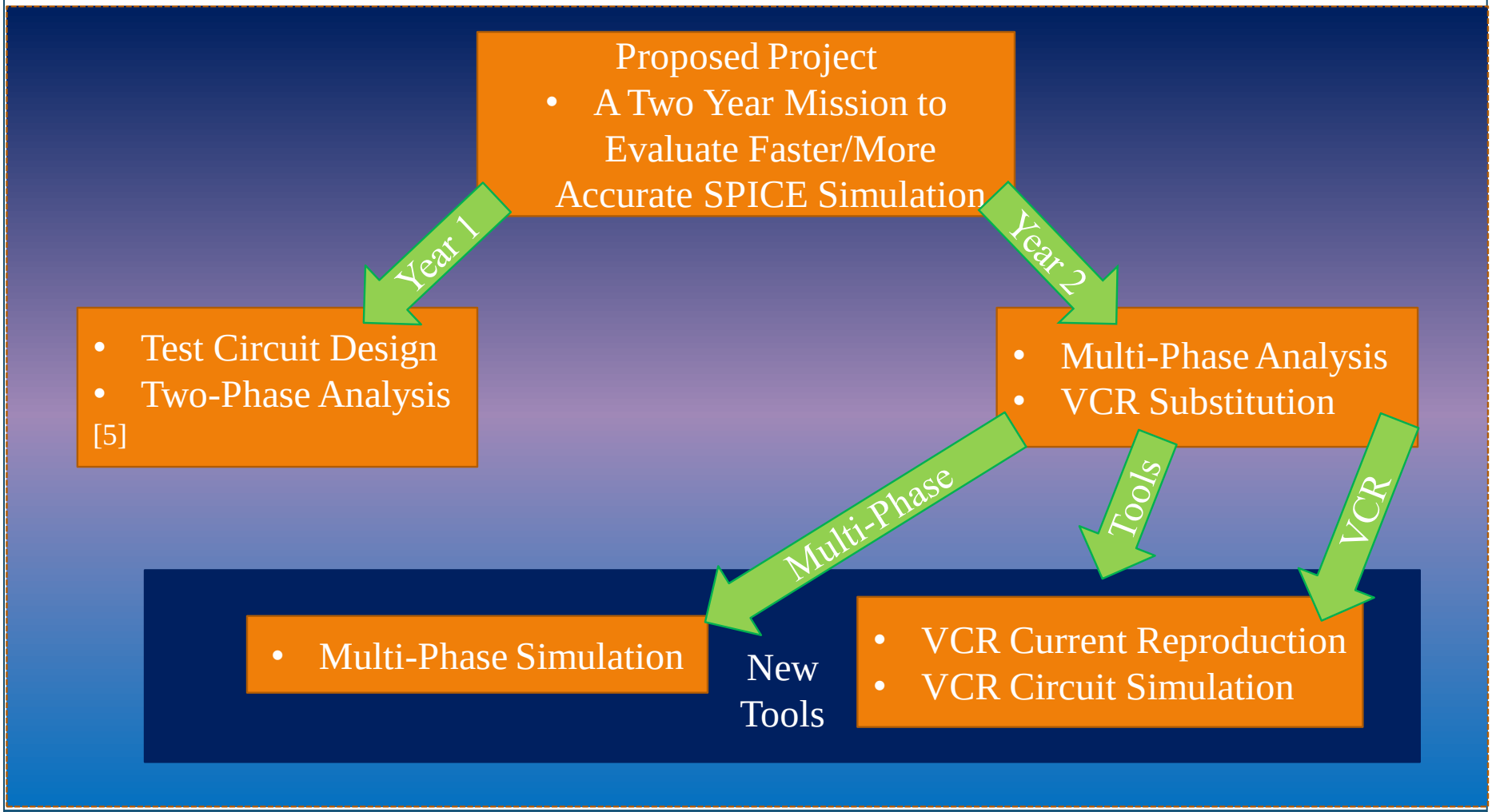


Phase 2 – VCR Subsitution



[3]

Simulation Tool Flow and Process Design



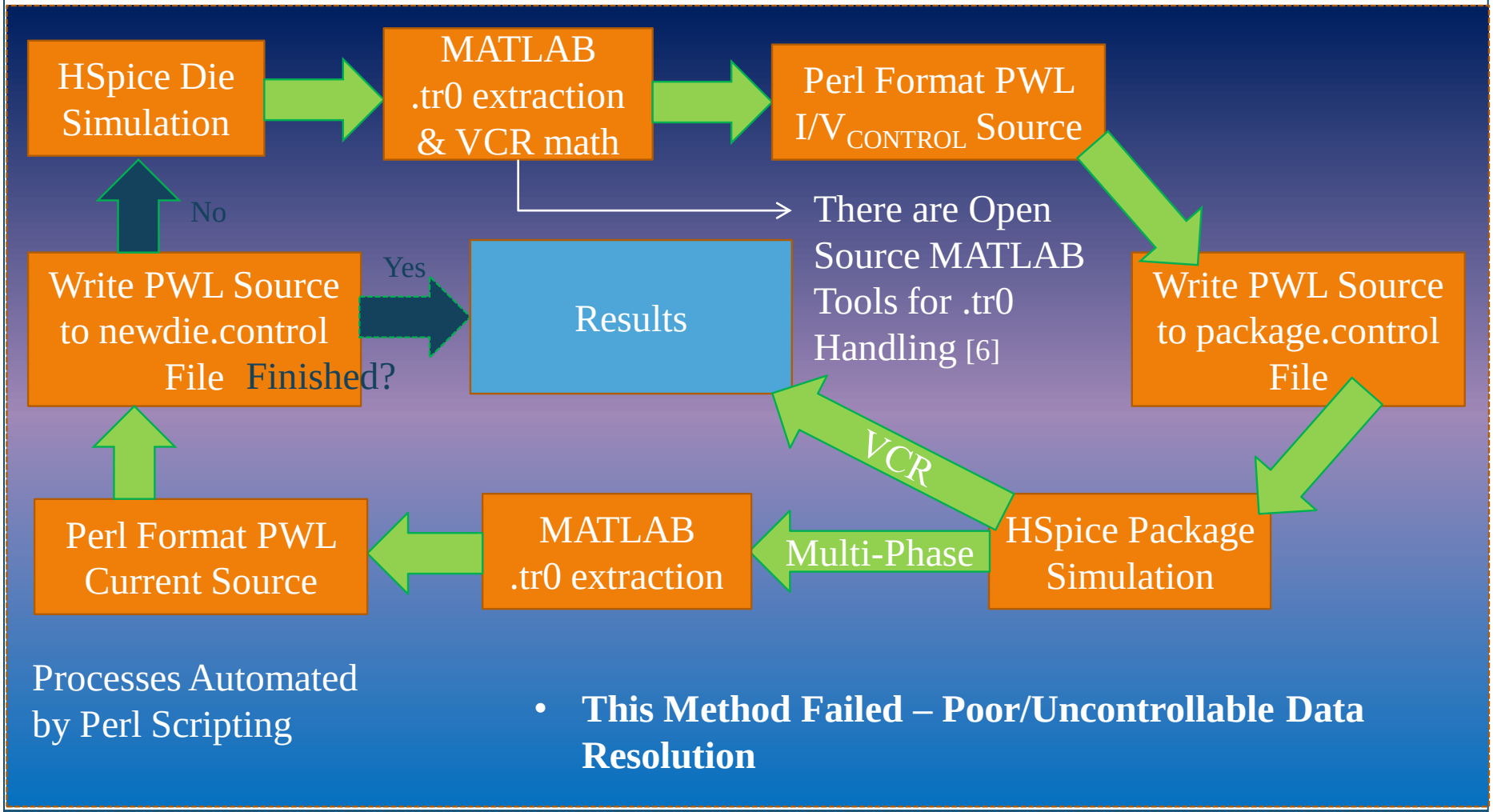
Initial Problems to Solve

- Tool Design
  - Both VCR and Multi-Phase are new techniques
  - Tools to perform these analyses need to be created
- Decisions to be Made
  - Simulator for base simulations
  - How the process should flow
  - Which data is important
  - How to implement the data as inputs

Base Simulator

- HSpice:
  - Industry “Gold Standard”
  - The simulator to use
- Why?
  - Much more precise, but takes longer to run
  - File outputs are much easier to work with
- Files:
  - .lis: text output; can command to contain signal data
  - .tr0: binary output; contains data for all signals

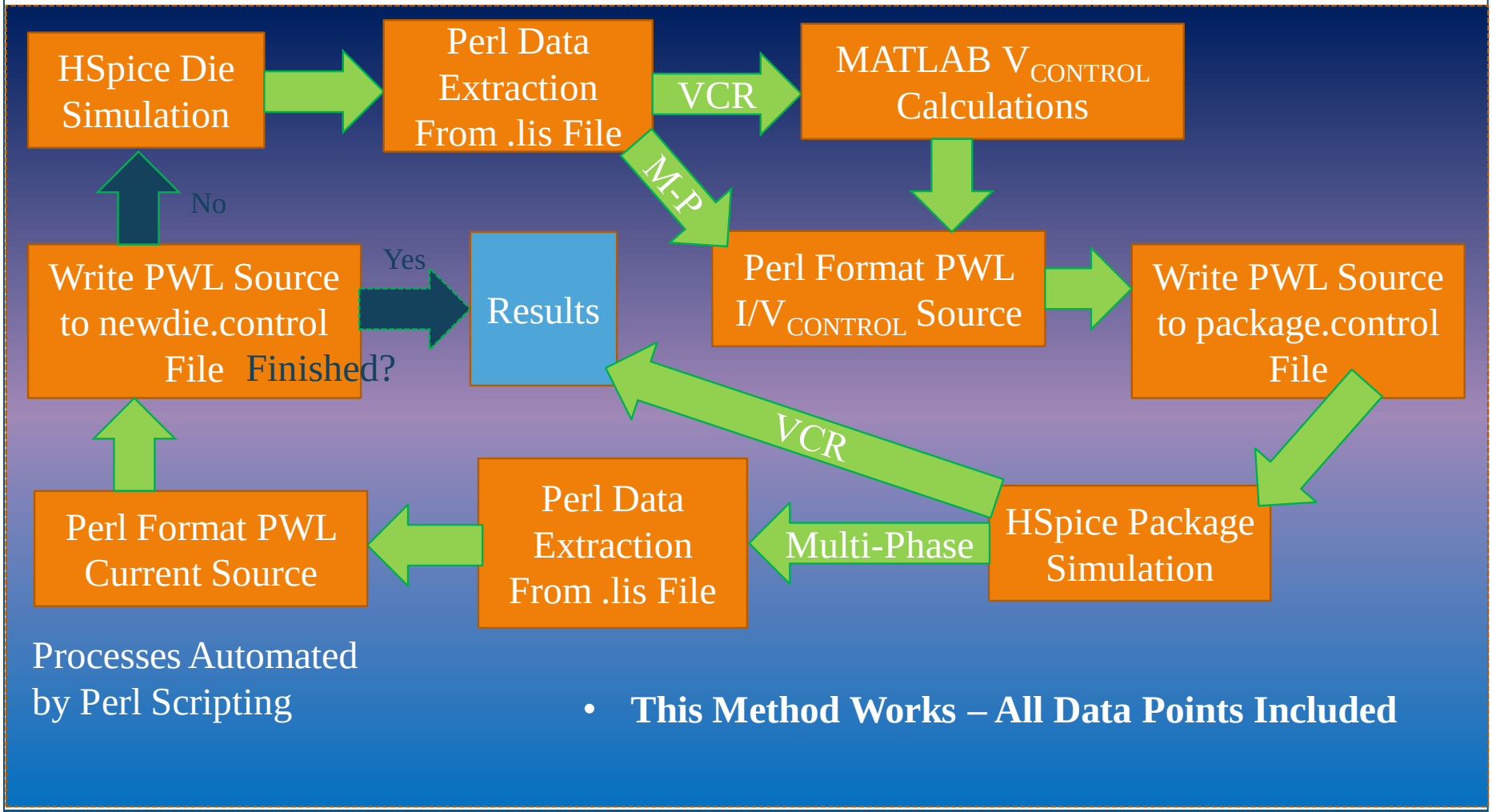
First Approach at Tool Flow



Processes Automated by Perl Scripting

- **This Method Failed – Poor/Uncontrollable Data Resolution**

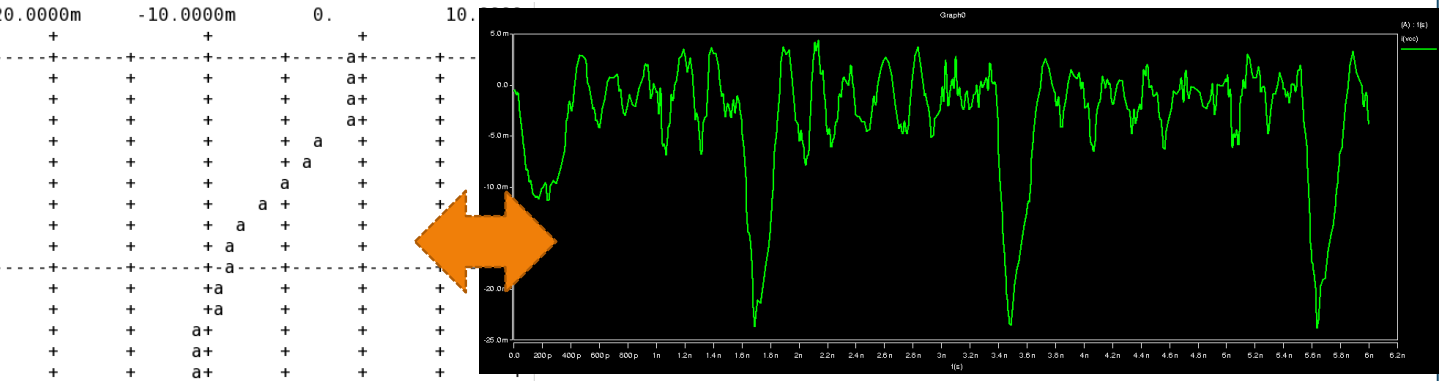
Second Approach at Tool Flow



Processes Automated by Perl Scripting

- **This Method Works – All Data Points Included**

Summary of Results



```
(a       )     -30.0000m     -20.0000m     -10.0000m       0.          10.
                     +             +             +             +
  0.       -578.225u-+------+------+------+------+------+------a+------+---
 10.0000p  -615.882u +      +      +      +      +      +     a+      +
 20.0000p  -927.340u +      +      +      +      +      +     a+      +
 30.0000p  -968.210u +      +      +      +      +      +     a+      +
 40.0000p    -2.557m +      +      +      +      +      +  a    +      +
 50.0000p    -3.652m +      +      +      +      +      + a    +      +
 60.0000p    -4.948m +      +      +      +      +      a      +      +
 70.0000p    -6.101m +      +      +      +      +    a +      +      +
 80.0000p    -7.581m +      +      +      +      +  a   +      +
 90.0000p    -8.321m +      +      +      +      + a    +      +
100.0000p    -8.705m-+------+------+------+------+-a----+------+------+---
110.0000p    -9.545m +      +      +      +      +a     +      +      +
120.0000p    -9.455m +      +      +      +      +a     +      +      +
130.0000p   -10.420m +      +      +      +     a+      +      +      +
140.0000p   -10.774m +      +      +      +     a+      +      +      +
150.0000p   -10.995m +      +      +      +     a+      +      +      +
160.0000p   -10.973m +      +      +      +     a+      +      +      +
170.0000p   -11.093m +      +      +      +    a +      +      +      +
180.0000p   -10.921m +      +      +      +     a+      +      +      +
190.0000p   -10.433m +      +      +      +     a+      +      +      +
200.0000p   -10.074m-+------+------+------+------a------+------+------+---
210.0000p    -9.862m +      +      +      +      a      +      +      +
220.0000p    -9.598m +      +      +      +      +a     +      +      +
230.0000p   -10.554m +      +      +      +     a+      +      +      +
```

```
VCC 0 POWER PWL(30.0000P 1.211 40.0000P 1.211
+ 50.0000P 1.208 60.0000P 1.203 70.0000P 1.202
+ 80.0000P 1.200 90.0000P 1.198 100.0000P 1.198
+ 110.0000P 1.197 120.0000P 1.197 130.0000P 1.196
+ 140.0000P 1.196 150.0000P 1.196 160.0000P 1.197
+ 170.0000P 1.198 180.0000P 1.200 190.0000P 1.201
+ 200.0000P 1.192 210.0000P 1.192 220.0000P 1.188
+ 230.0000P 1.190 240.0000P 1.191 250.0000P 1.193
+ 260.0000P 1.195 270.0000P 1.197 280.0000P 1.200
+ 290.0000P 1.201 300.0000P 1.203 310.0000P 1.203
+ 320.0000P 1.204 330.0000P 1.204 340.0000P 1.203
+ 350.0000P 1.202 360.0000P 1.202 370.0000P 1.216
+ 380.0000P 1.210 390.0000P 1.208 400.0000P 1.207
+ 410.0000P 1.204 420.0000P 1.202 430.0000P 1.200
+ 440.0000P 1.198 450.0000P 1.197 460.0000P 1.197
+ 470.0000P 1.196 480.0000P 1.197 490.0000P 1.198
+ 500.0000P 1.198 510.0000P 1.199 520.0000P 1.200
+ 530.0000P 1.201 540.0000P 1.202 550.0000P 1.201
+ 560.0000P 1.191 570.0000P 1.190 580.0000P 1.186
+ 590.0000P 1.189 600.0000P 1.190 610.0000P 1.193
+ 620.0000P 1.197 630.0000P 1.200 640.0000P 1.203
+ 650.0000P 1.205 660.0000P 1.205 670.0000P 1.206
+ 680.0000P 1.205 690.0000P 1.203 700.0000P 1.202
+ 710.0000P 1.201 720.0000P 1.200 730.0000P 1.215
+ 740.0000P 1.210 750.0000P 1.208 760.0000P 1.208
+ 770.0000P 1.205 780.0000P 1.203 790.0000P 1.201
+ 800.0000P 1.199 810.0000P 1.197 820.0000P 1.197
```

Review

- New SPICE Simulation Strategies Beneficial to Circuit Design
- New Simulation Strategies Require New Tool Designs to Work
- HSpice Allows Tools to be Crafted Using its Outputs
- My Contribution Was to Design and Create the Tools
- Tools Created that Made Multi-Phase and VCR Analyses Possible

Questions?

- Contact:

  e.michal.peterson@utah.edu

- References:

[1] MMX, “Motorola Xoom Tablet | Uncrate”, http://www.uncrate.com/men/gear/laptops/motorola-xoom-tablet/ - accessed 3/2011

[2] Ziff Davis Inc., “Verizon removes Skype http://www.geek.com/articles/mobile/verizon-removes-skype-video-from-htc-thunderbolt-20110218/ - accessed 3/2011

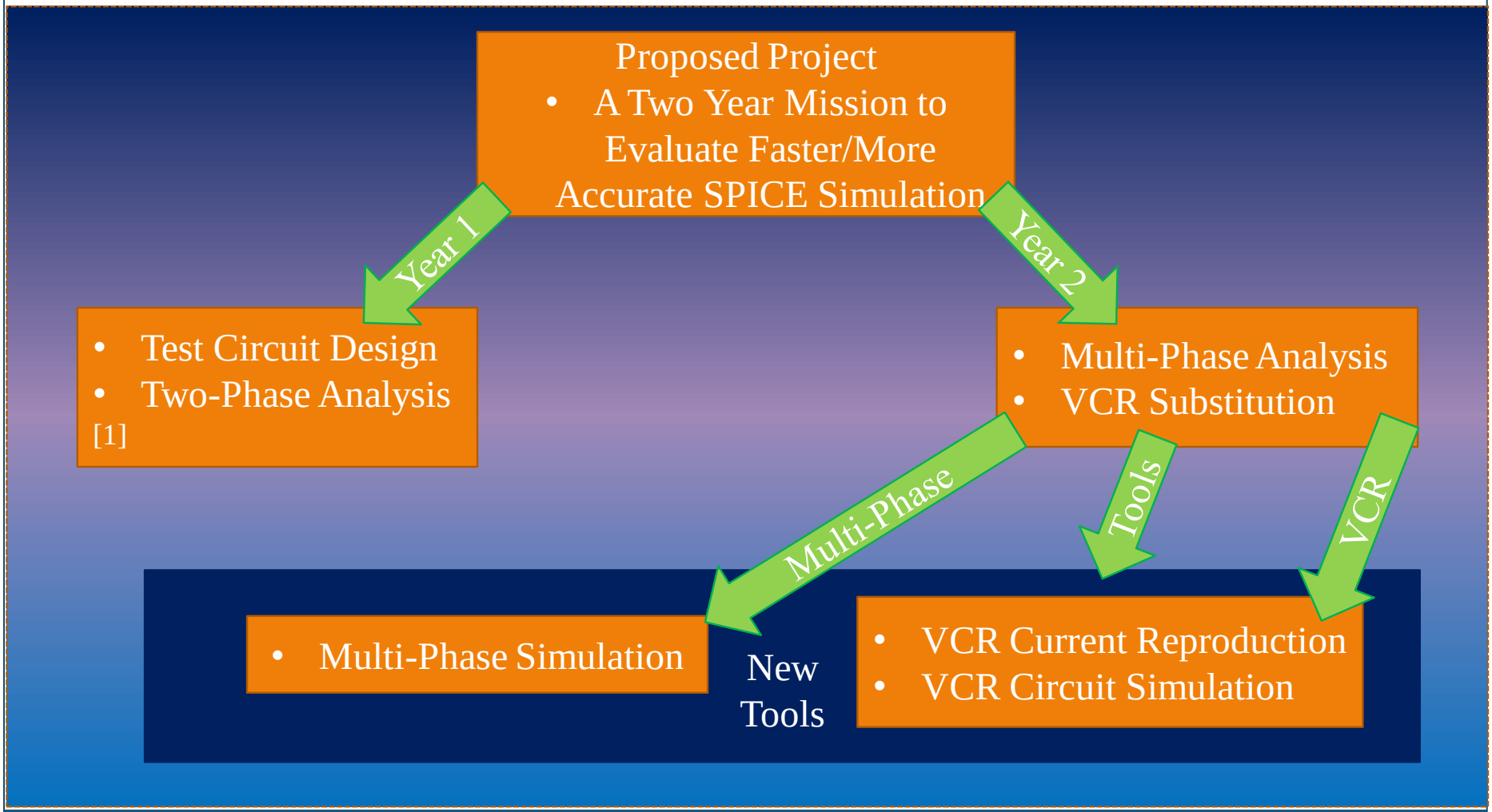
[3] Hollis, T., "University of Utah Senior Clinic 2009-2010". [PowerPoint Presentation]. April 10, 2009.

[4] Synopsis Corporation, “HSPICE”, http://www.synopsys.com/Tools/Verification/AMSVerification/CircuitSimulation/HSPICE/Pages/default.aspx - accessed 3/2011

[5] 2009-2010 Micron Clinic Team, “Evaluation of Integrated Circuit Power Supply Noise with Two-Phase Analysis”, April 2009

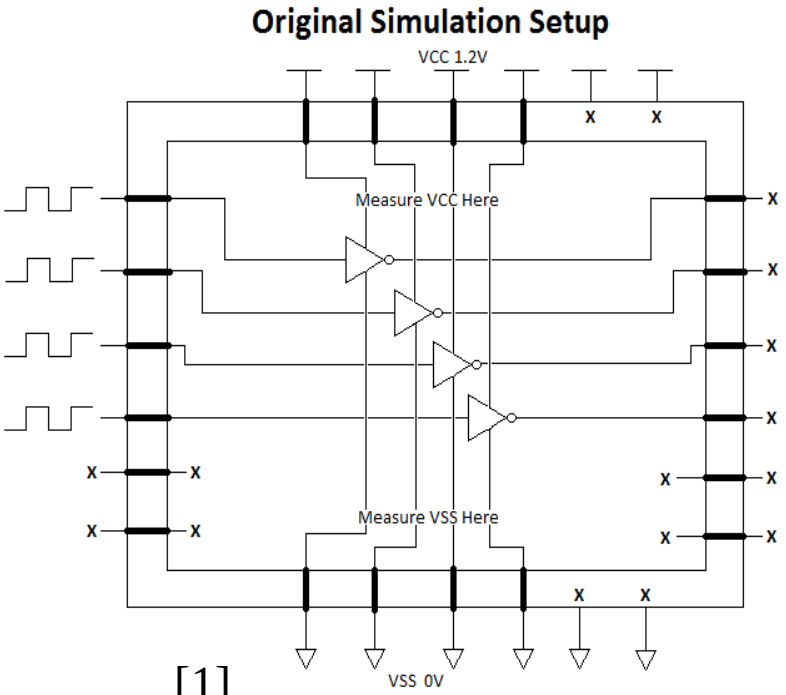
[6] Perrott, M.H. “CAD Tools of Michael H. Perrott and former students”, http://www.cppsim.com/download_hspice_tools.html, accessed 3/2011

Multi-Phase Measurements and Analysis



Goals for Multi-Phase Approach

- Separation of Single Simulation
  - Replace internal die with varying current source
- Less Accuracy/Shorter Run Times
  - Single iteration
- More Accuracy/Longer Run Times
  - Multiple iterations
  - Determine if converging
- Simple Circuits Combine to Form Larger



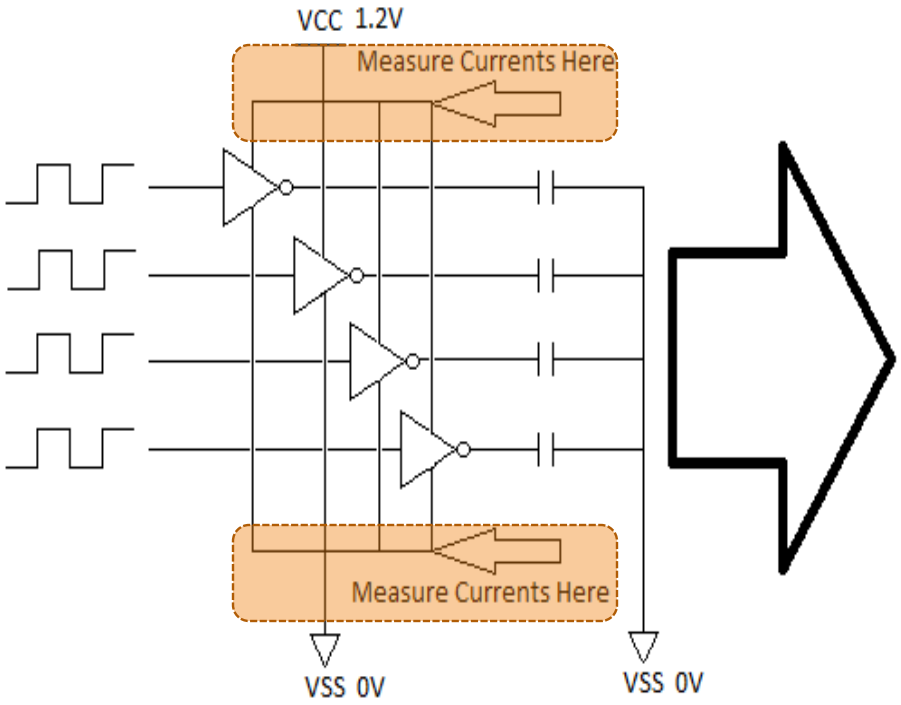
[1]

Multi-Phase Method Introduction

- HSIM^{plus} versus HSpice
  - HSIM^{plus}: faster run times [1]
  - HSpice: more accuracy, industry standard [1]
- HSpice for All Multi-Phase Simulations
- Circuits Simulated [1]
  - Four-Inverter Circuit
  - 16-bit Adder
  - 8-bit Multiplier
  - 4-stage, 8-stage, 16-stage Fibonacci Sequence

Multi-Phase Implementation

- First Phase Captures Rail Currents



- From: Ideal Current Source

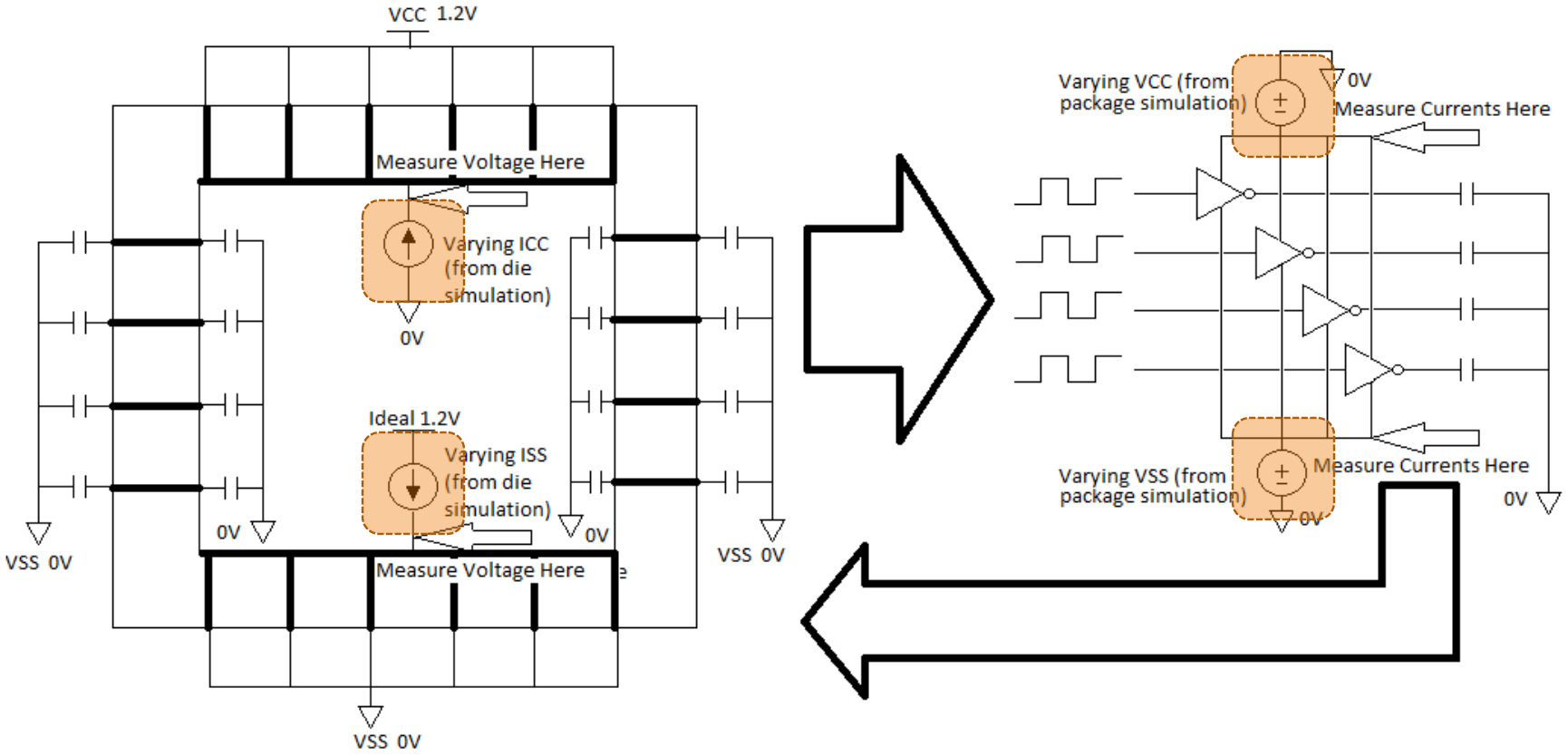
```
ICC POWER 0 PULSE(0 50U 1N 2N)
ISS GND0 IDEAL PULSE(0 5U 1N 2N)
```

- To: PWL Current Source

```
ICC POWER 0 PWL(0. -102.682U 10.0000P -5.885M
+ 20.0000P -4.712M 30.0000P -4.715M 40.0000P -4.627M
+ 50.0000P -4.361M 60.0000P -4.197M 70.0000P -4.420M
+ 80.0000P -4.343M 90.0000P -4.364M 100.0000P -4.506M
+ 110.0000P -4.428M 120.0000P -4.523M 130.0000P -4.453M
+ 140.0000P -4.541M 150.0000P -4.529M 160.0000P -4.617M
+ 170.0000P -4.630M 180.0000P -4.688M 190.0000P -4.584M
+ 200.0000P 1.440M 210.0000P -290.962U 220.0000P 145.015U
+ 230.0000P -262.599U 240.0000P -218.916U 250.0000P -269.011U
+ 260.0000P -250.744U 270.0000P -256.273U 280.0000P -368.764U
+ 290.0000P -134.614U 300.0000P -294.786U 310.0000P -58.754U
+ 320.0000P -139.628U 330.0000P -62.595U 340.0000P 14.458U
+ 350.0000P 14.801U 360.0000P -65.145U 370.0000P -7.115M
+ 380.0000P -4.079M 390.0000P -4.566M 400.0000P -4.477M
+ 410.0000P -4.285M 420.0000P -4.356M 430.0000P -4.323M
+ 440.0000P -4.303M 450.0000P -4.363M 460.0000P -4.450M
+ 470.0000P -4.365M 480.0000P -4.531M 490.0000P -4.552M
+ 500.0000P -4.490M 510.0000P -4.570M 520.0000P -4.585M
+ 530.0000P -4.606M 540.0000P -4.627M 550.0000P -4.464M
+ 560.0000P 1.471M 570.0000P -259.729U 580.0000P 104.648U
+ 590.0000P -375.821U 600.0000P -253.673U 610.0000P -372.869U
+ 620.0000P -418.878U 630.0000P -322.744U 640.0000P -280.595U
+ 650.0000P -175.229U 660.0000P -69.271U 670.0000P -130.621U
+ 680.0000P 18.685U 690.0000P 61.544U 700.0000P -35.062U
```

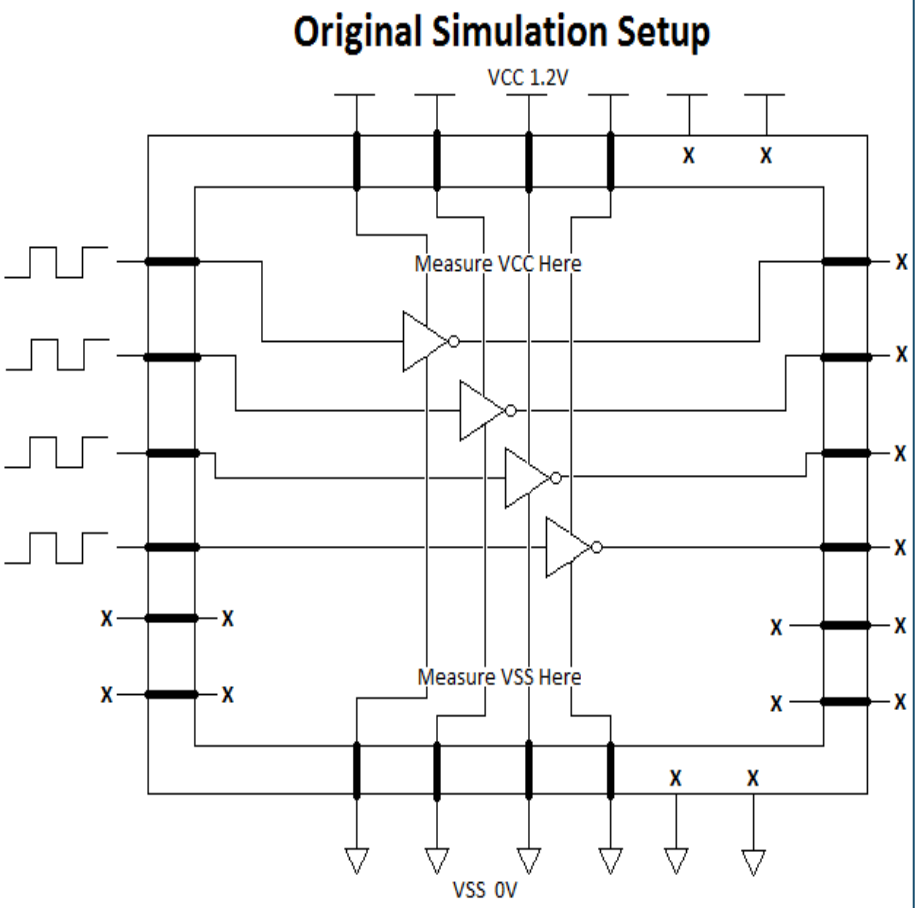
Multi-Phase Implementation

- Second Phase
- Third Phase Replaces First



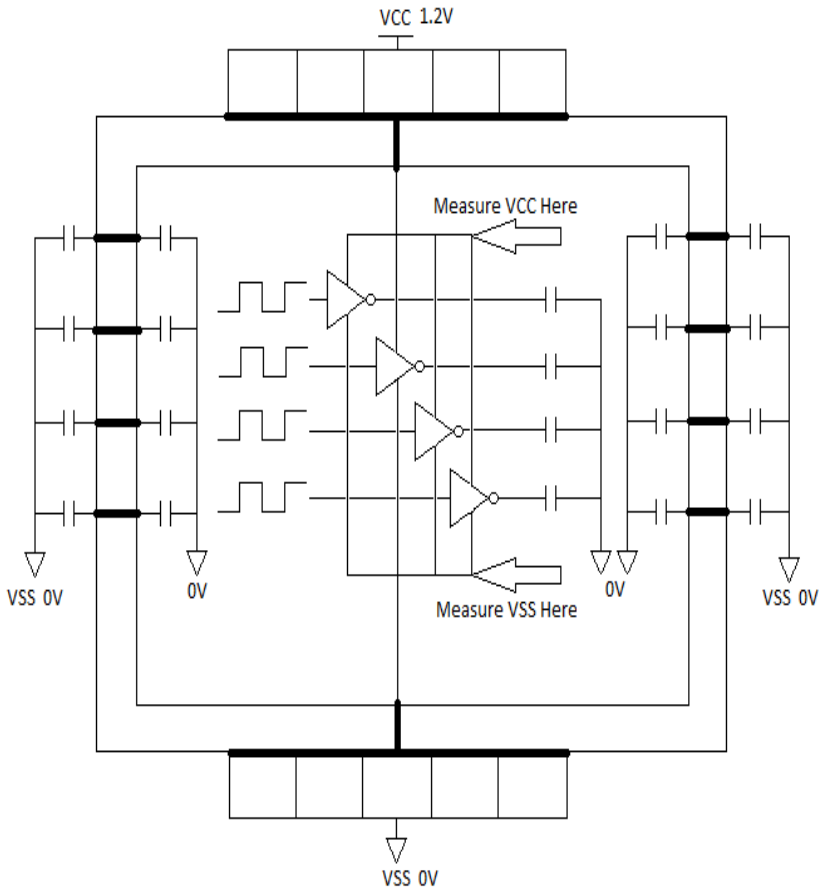
Original Combined Circuit Setup

- Baseline Circuit Problems
  - Mutual inductances [2]
  - Floating nodes
  - Modeling signals difficult
  - Signal voltage levels too low
  - Power voltage levels too low
  - Power voltage nodes vary

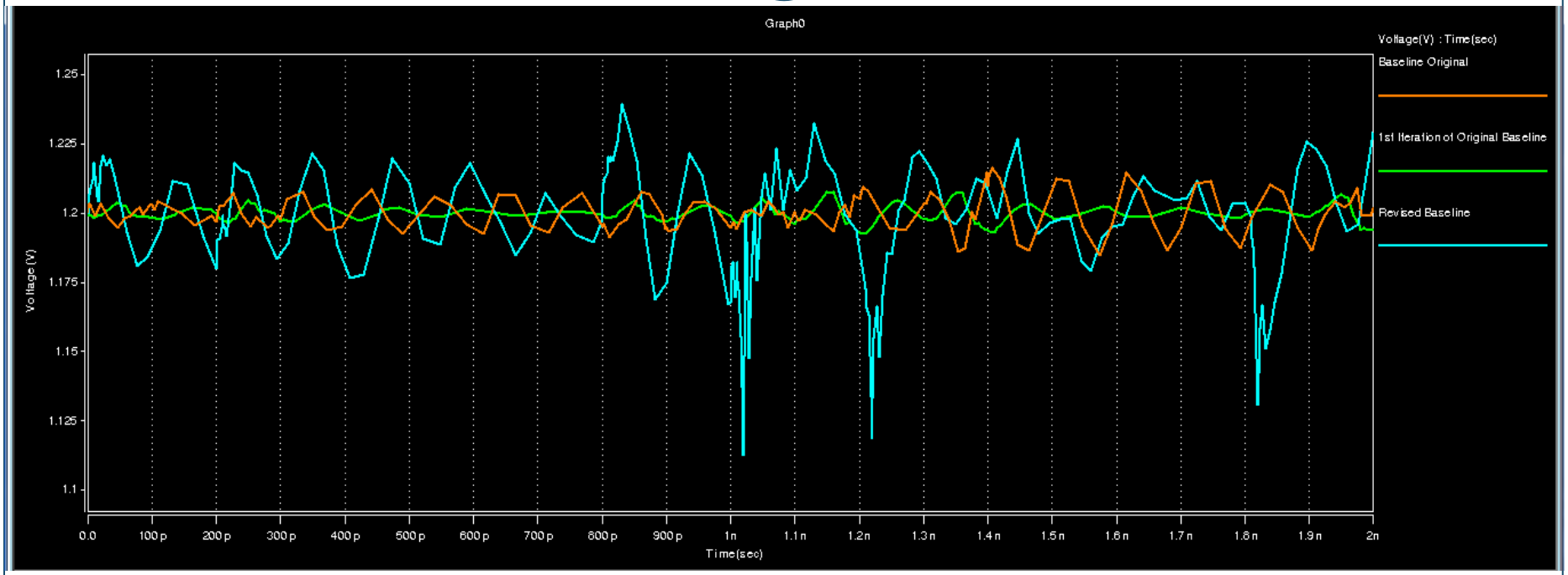


Revised Baseline HSpice Circuit

- Baseline Circuit Changes
  - Inputs/outputs to capacitance loads
  - Power nodes connected together
  - Ground nodes connected together
  - Signals inputs internal
  - Signal outputs to capacitance loads



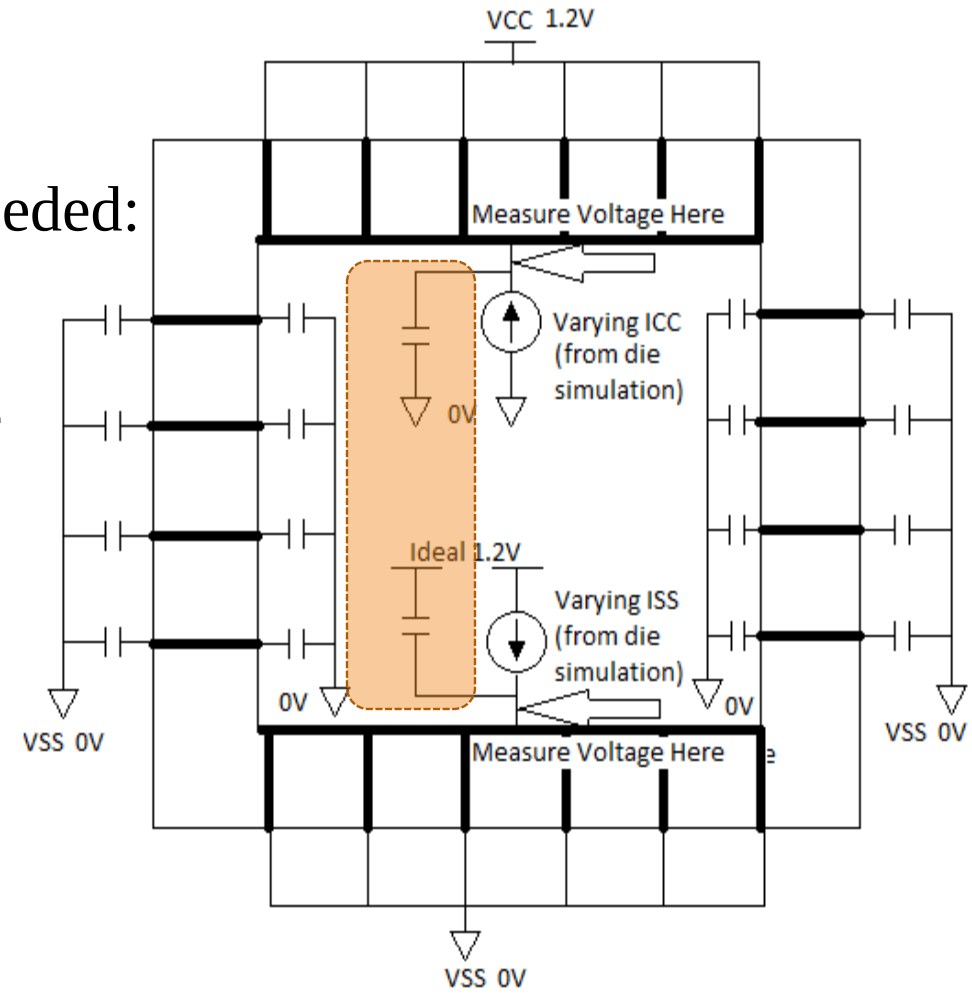
4-Inverter Original Circuit vs. Revised Circuit



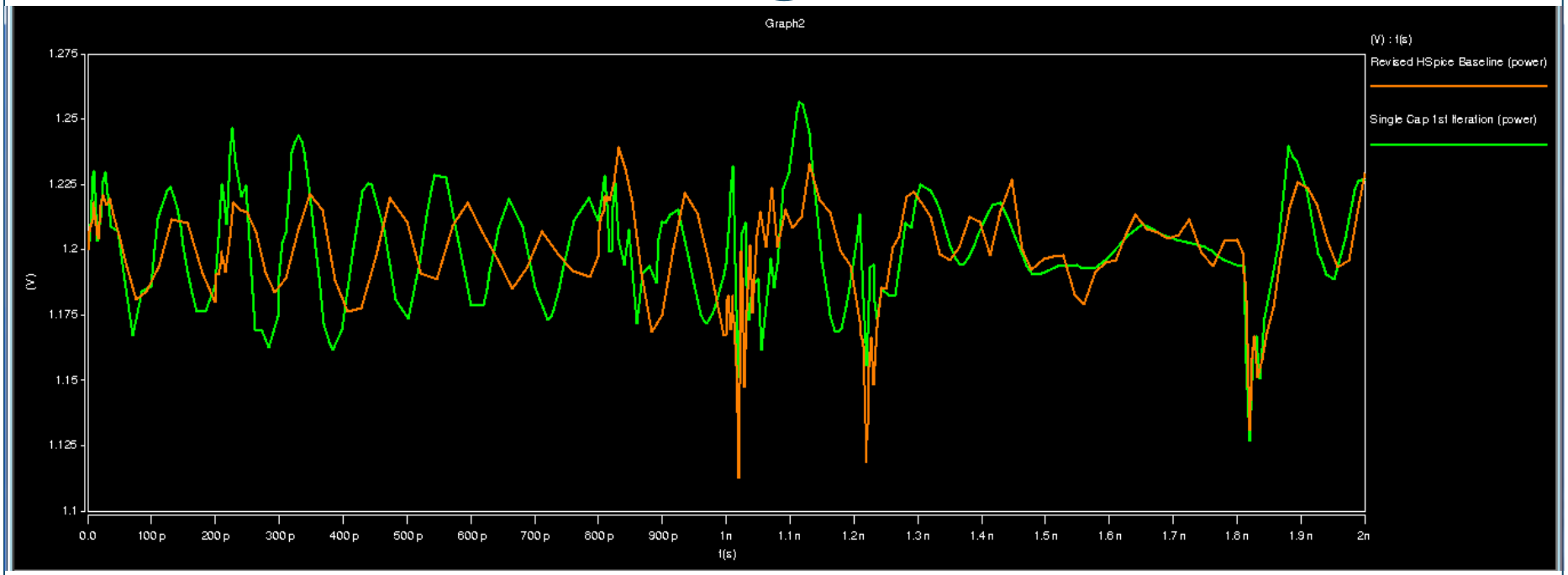
- Original HSpice Baseline Simulation (Orange)
- Original Circuit Multi-Phase 1st Iteration (Green)
- Revised HSpice Baseline Simulation (Blue)

Multi-Phase Intermediate Results

- Current Source Not Suitable Circuit Replacement
- Second Phase Modification Needed:
  - Capacitor load for power node
  - Capacitor load for ground node

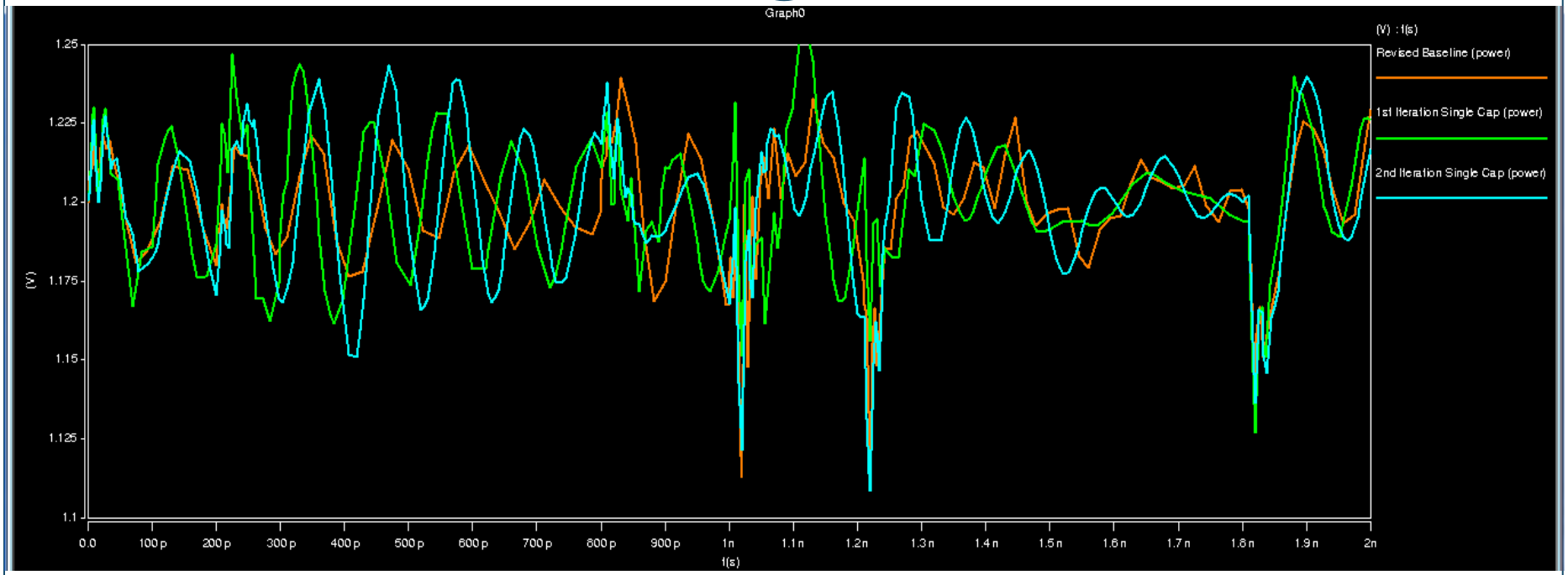


4-Inverter Multi-Phase Results



- Revised HSpice Baseline Simulation (Orange)
- Multi-Phase 1st Iteration (Green)
  - Single Coupling capacitor of 100pF

4-Inverter Multi-Phase Results



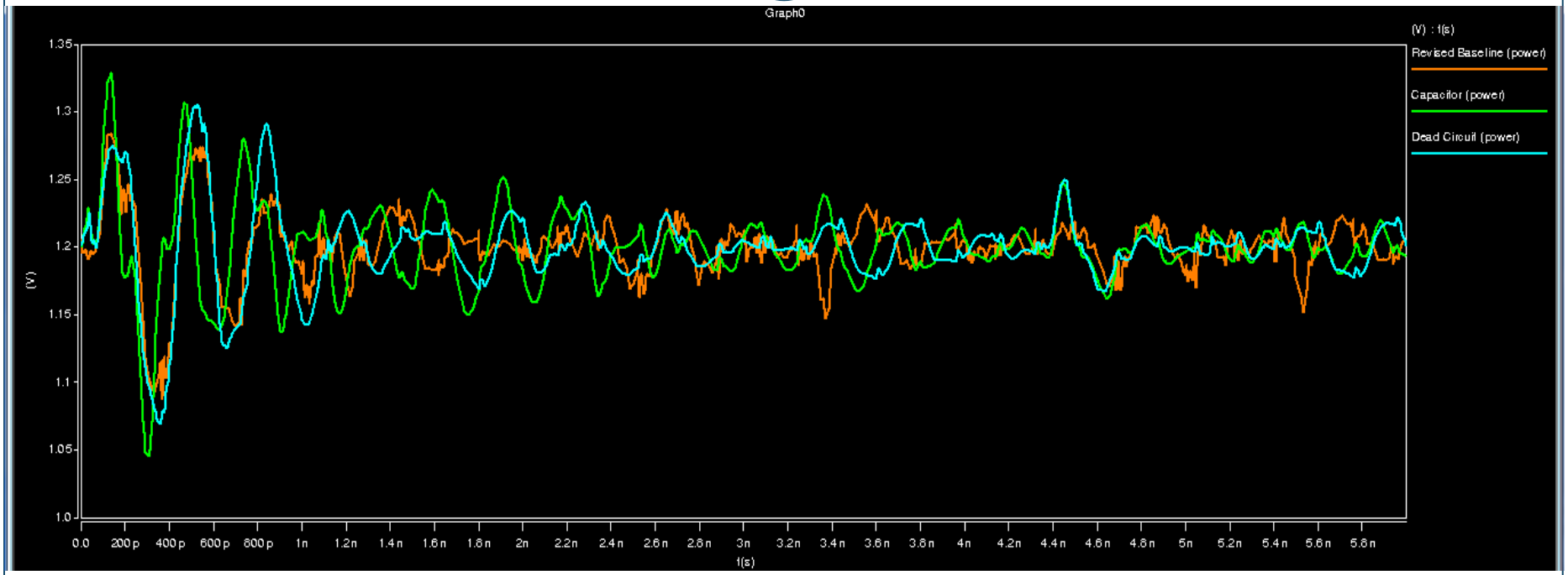
- Revised HSpice Baseline Simulation (Orange)
- Multi-Phase 1st Iteration (Green) , Single 100pF Capacitor
- Multi-Phase 2nd Iteration (Blue) , Single 100pF Capacitor

Simulation Times for 4-Inverter Circuit

- With Single Capacitor

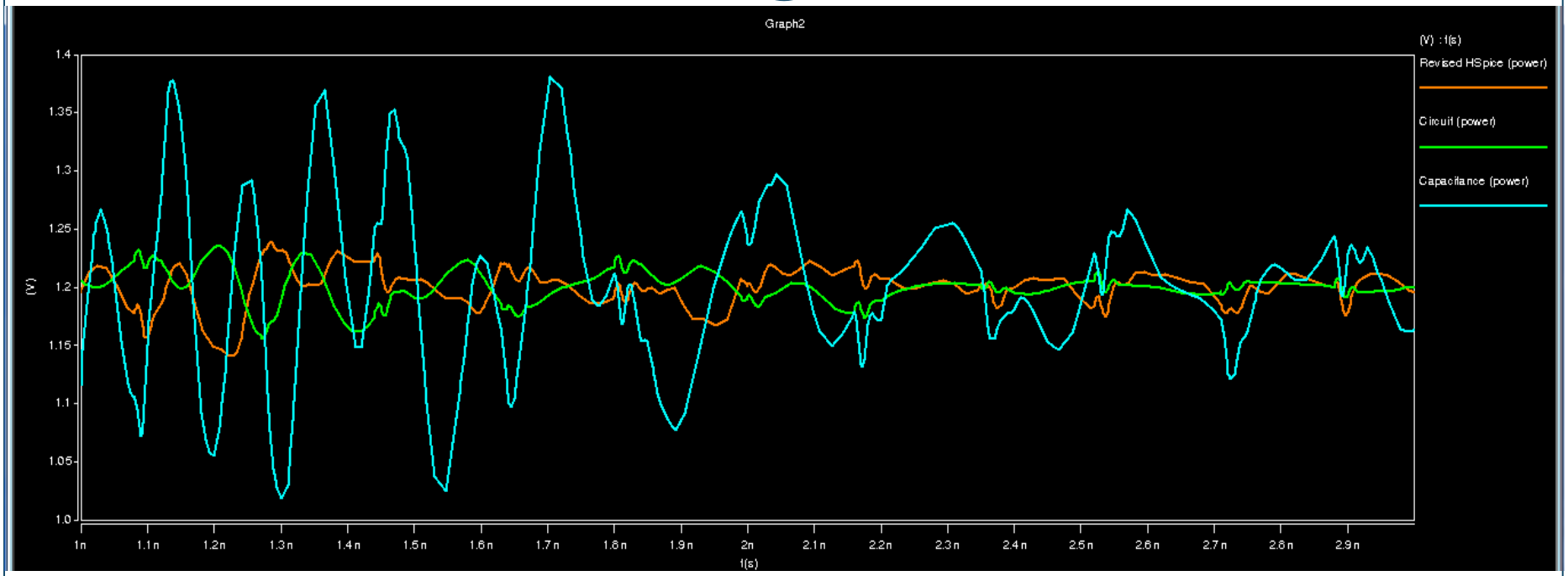
	Inverter (in seconds)			
	REAL TIME	USER TIME	SYSTEM TIME	LEVEL
HSIM^{plus}	-----	**44.30**	-----	-----
HSpice Package + Die	20.77	**19.29**	0.08	10
End of Iteration 1	16.32	**15.21**	0.09	10
End of Iteration 2	23.05	**22.66**	0.07	10
End of Iteration 3	21.46	21.06	0.12	10
End of Iteration 4	22.18	21.76	0.1	10
End of Iteration 5	24.66	23	0.11	10
End of Iteration 6	24.85	24.4	0.1	10
End of Iteration 7	25.9	24.37	0.1	10
End of Iteration 8	25.17	24.74	0.1	10
End of Iteration 9	27.14	25.68	0.1	10
End of Iteration 10	29	28.53	0.11	10

16-bit Adder Circuit



- Revised HSpice Baseline Simulation (Orange)
- Multi-Phase 1st Iteration with Capacitor (Green)
- Multi-Phase 1st Iteration with Circuit (Blue)

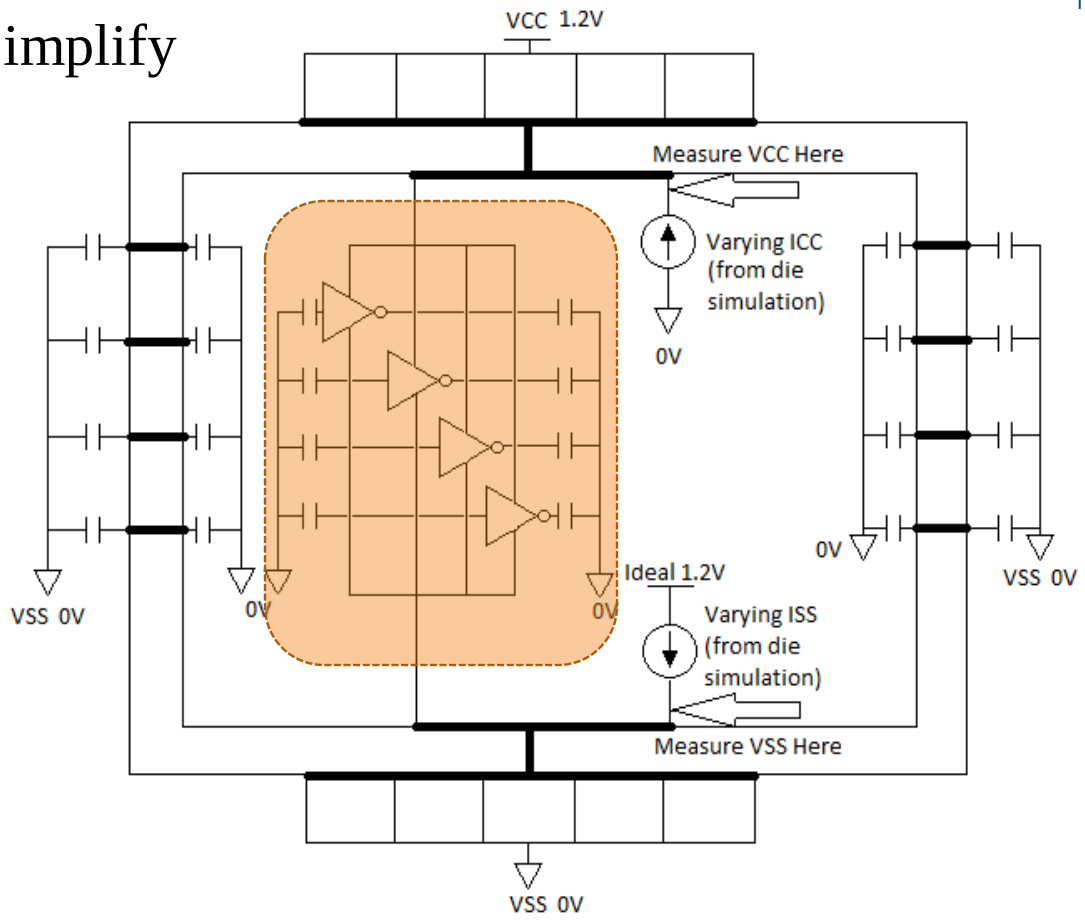
4-Stage Fibonacci Circuit



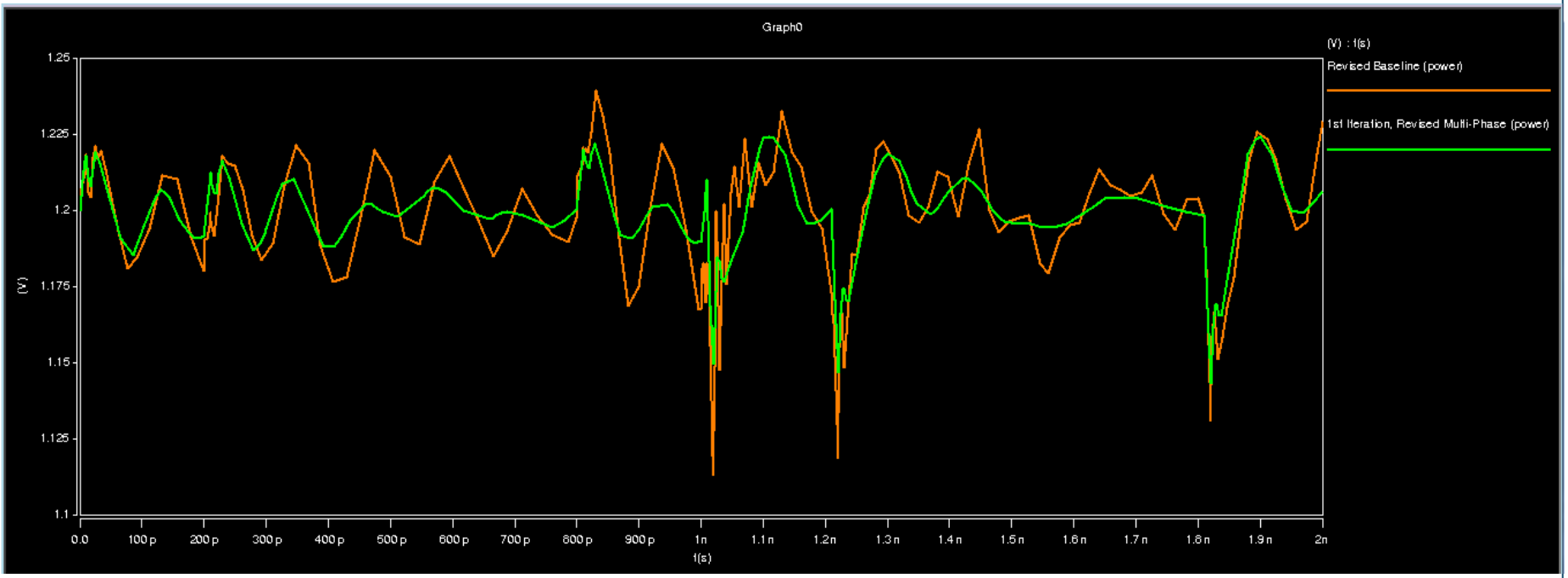
- Revised HSpice Baseline Simulation (Orange)
- Multi-Phase 1st Iteration (Green) with Circuit
- Multi-Phase 1st Iteration (Blue) with Capacitor

Revised Second Phase Circuit

- Problem:
  - Large Circuits Do Not Simplify
- Solution:
  - Replace single cap for entire circuit
- Predictions:
  - Longer run times, more to calculate
  - Waveforms Closer to Baseline Values

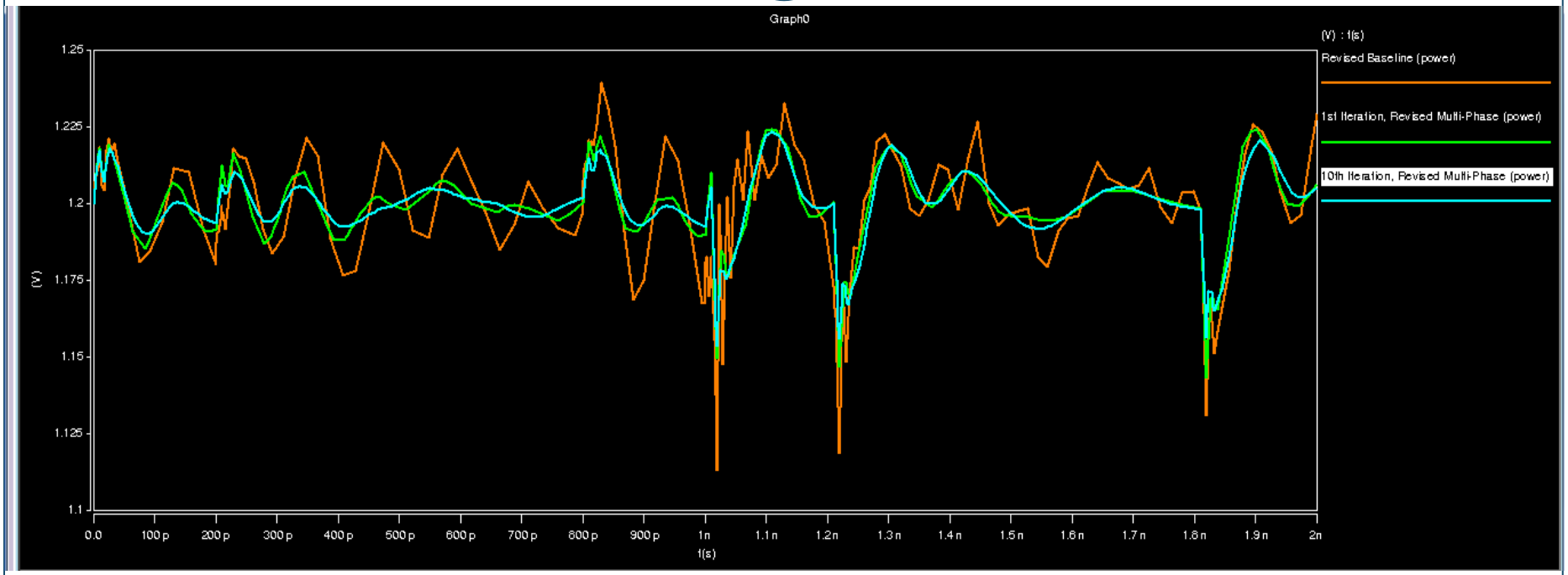


Multi-Phase Results with Capacitance Circuit



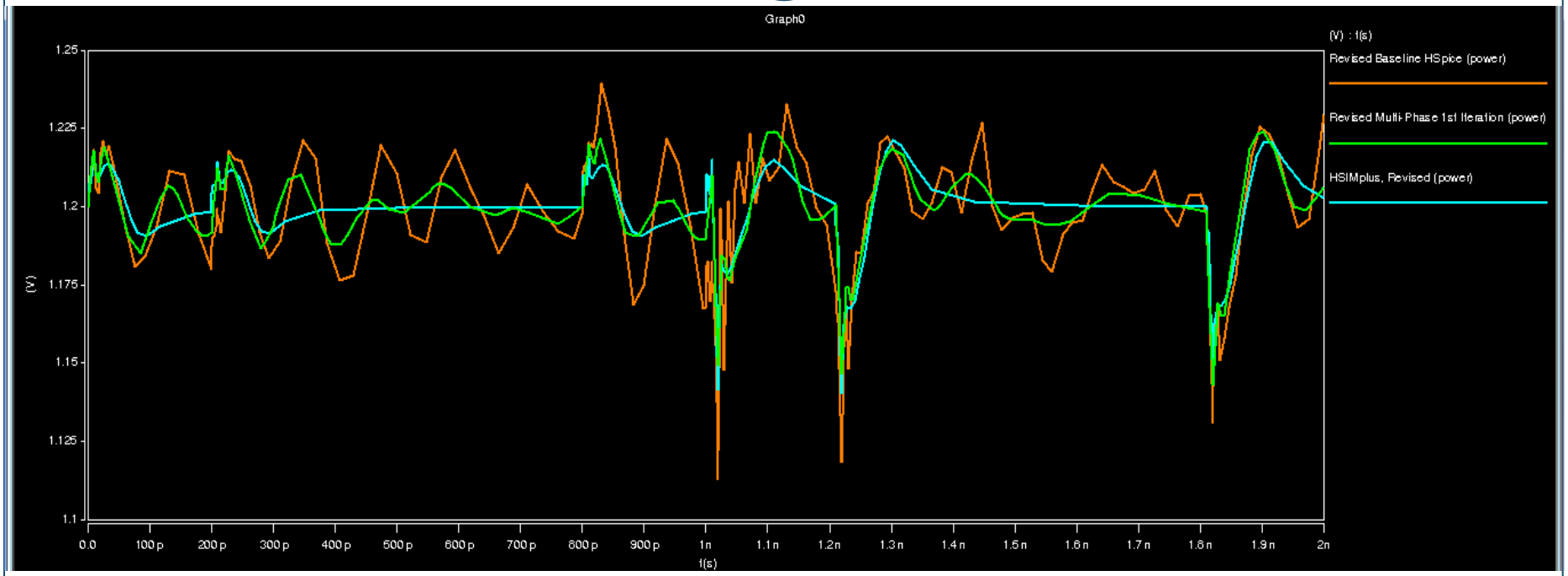
- Revised HSpice Baseline 4-Inverter Simulation (Orange)
- Revised 4-Inverter Multi-Phase 1st Iteration (Green)
  - Circuit included in second phase

Multi-Phase Results with Capacitance Circuit



- Revised HSpice Baseline 4-Inverter Simulation (Orange)
- 4-Inverter Multi-Phase 1st Iteration (Green) with Circuit
- 4-Inverter Multi-Phase 10th Iteration (Blue) , with Circuit

HSPICE, HSIM^{plus}, and Multi-Phase Comparison



- Revised HSpice Baseline Simulation (Orange)
- Multi-Phase 1st Iteration with Circuit (Green)
- HSIM^{plus} Revised Baseline Simulation(Blue)

Simulation Times for 4-Inverter Circuit

- With Capacitance Network

	Inverter (in seconds)			
	REAL TIME	USER TIME	SYSTEM TIME	INTERVAL (ps)
HSIM^{plus}	-------	**44.30**	------	-------
HSpice Package + Die	20.77	**19.29**	0.08	10
End of Iteration 1	38.06	**36.68**	0.1	10
End of Iteration 2	49.35	47.12	0.09	10
End of Iteration 3	46.1	45.34	0.08	10
End of Iteration 4	49.76	45.36	0.11	10
End of Iteration 5	53.89	46.57	0.07	10
End of Iteration 6	47.23	46.37	0.06	10
End of Iteration 7	47.93	46.4	0.08	10
End of Iteration 8	47.93	46.4	0.08	10
End of Iteration 9	49.52	45.48	0.07	10
End of Iteration 10	46.01	45.07	0.05	10

Simulation Times for Other Circuits

- With capacitance network

	Adder (in seconds)			
	REAL TIME	**USER TIME**	**SYSTEM TIME**	**INTERVAL (ps)**
HSIM^{plus}	-------	**164.07**	-------	10
HSpice Package + Die	78.05	**76.7**	1.13	10
Capacitive Circuit 1	153.2	**145.57**	0.44	10
Capacitive Circuit 2	198.65	193.3	1.6	10
Capacitive Circuit 3	221.96	218.34	1.83	10

	Multiplier (in seconds)			
	REAL TIME	**USER TIME**	**SYSTEM TIME**	**INTERVAL (ps)**
HSIM^{plus}	-------	**158.92**	-------	10
HSpice Package + Die	132.14	**131.08**	0.87	**10**
Capacitive Circuit 1	166.88	**160.81**	0.89	10
Capacitive Circuit 2	189.54	186.52	1.64	10
Capacitive Circuit 3	196.1	193.39	1.36	10

Simulation Times for Other Circuits

- With capacitance network

	Fibonacci 4-stage (in seconds)			
	REAL TIME	USER TIME	SYSTEM TIME	INTERVAL (ps)
HSIM^{plus}	-------	**161.8**	-------	**10**
HSpice Package + Die	117.83	**117.05**	1.1	**10**
Capacitive Circuit 1	222.62	**209.28**	1.8	10
Capacitive Circuit 2	218.26	218.26	1.17	10
Capacitive Circuit 3	240.19	236.9	1.35	10

	Fibonacci 8-stage (in seconds)			
	REAL TIME	USER TIME	SYSTEM TIME	INTERVAL (ps)
HSIM^{plus}	-------	**235.44**	-------	**10**
HSpice Package + Die	200.4	**199.5**	0.45	**10**
Capacitive Circuit 1	344.65	**342.28**	1.48	10
Capacitive Circuit 2	654.23	632.29	2.65	10

	Fibonacci 16-stage (in seconds)			
	REAL TIME	USER TIME	SYSTEM TIME	INTERVAL (ps)
HSIM^{plus}	-------	**408.47**	-------	**10**
HSpice Package + Die	321.16	**314.21**	1.2	**10**
Capacitive Circuit 1	1142.47	**1138.84**	1.23	10
Capacitive Circuit 2	2848.44	2839.49	6.22	10

Baseline Simulations Time Comparison

	4-INVERTER					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	18,176	18,208	18,208	18,208	21,632	
Time (in seconds)	20.696	20.684	20.706	20.766	43.958	19.29

	16-BIT ADDER					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	488,008	485,562	544,118	543,272	1,959,856	
Time (in seconds)	164.43	164.32	168.47	164.53	343.5	76.7

	8-BIT MULTIPLIER					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	7,447,602	7,450,026	7,526,926	7,461,290	10,113,416	
Time (in seconds)	298.03	294.91	303.61	294.08	621.24	131.08

Baseline Simulations Time Comparison

	4-STAGE FIBONACCI					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	2,115,926	2,121,662	2,193,106	2,233,582	7,450,784	
Time (in seconds)	161.33	163.87	164.3	160.91	350.48	117.05

	8-STAGE FIBONACCI					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	5,801,828	5,794,150	5,926,943	6,006,732	20,997,664	
Time (in seconds)	227.73	226.36	230.58	227.69	495.74	199.5

	16-STAGE FIBONACCI					
HSIMplus Precision	**Level 0**	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**HSpice**
MOS evaluations	22,216,158	22,667,222	22,017,499	22,584,616	74,063,680	
Time (in seconds)	405.72	408.4	409.02	407.29	940.17	314.21

Conclusions

- Current Source Not a Simple Circuit Drop-in Replacement
- Single Capacitance:
  - Time decreased for single iteration
  - Multiple iterations converged to HSIM^{plus} values
  - Multiple iterations for larger circuits diverged
- Capactance Network:
  - Time increased dramatically for single iteration
  - Performance increased compared to single capacitance

Questions?

- Contact:

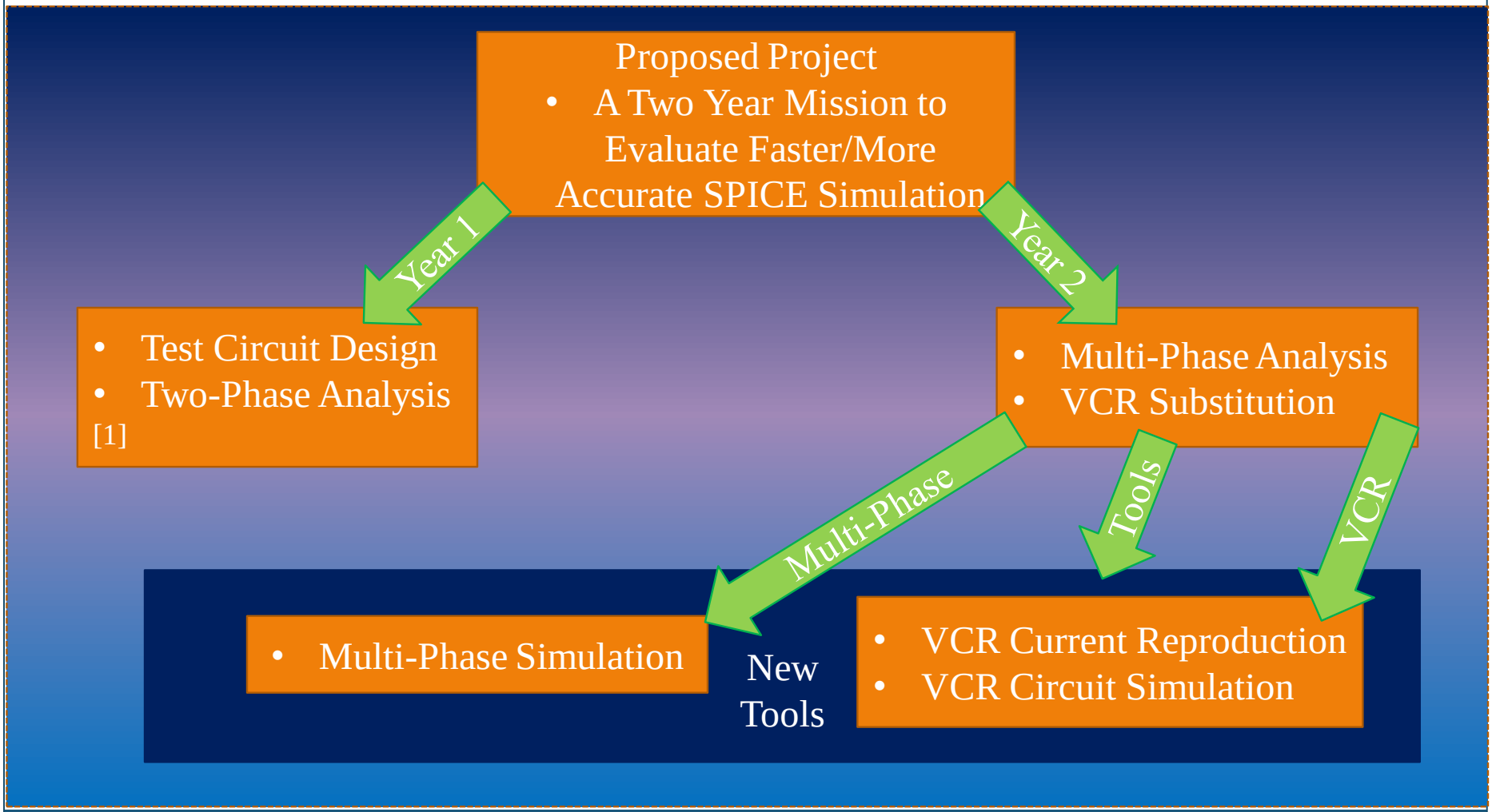
  thomas.white@utah.edu

- References:

[1] 2009-2010 Micron Clinic Team, “Evaluation of Integrated Circuit Power Supply Noise with Two-Phase Analysis”, April 2009

[2] Hollis, Tim, "University of Utah Senior Clinic 2009-2010". [PowerPoint Presentation]. April 10, 2009.

Recreating Currents Using Voltage-Controlled Resistors



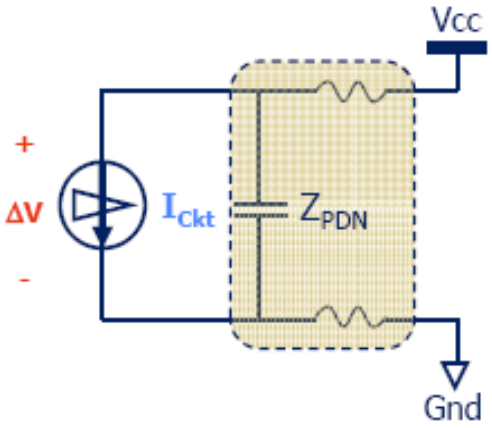
Overview

- Two-Phase Model
- Voltage-Controlled Resistor (VCR)
- Current Generating Circuit
- Simulation Results

Two-Phase Analysis

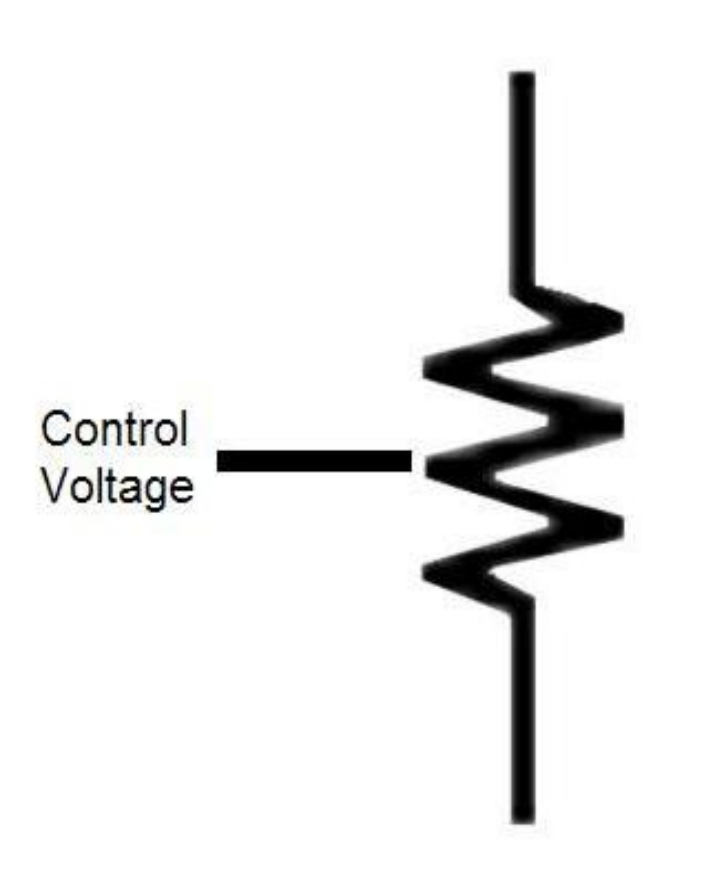
Phase 1:
Run time-domain simulation with all circuitry in place and capture circuit-specific currents into and out of the supplies

Phase 2:
Apply extracted currents to full Power Delivery Network and capture static and dynamic voltage changes



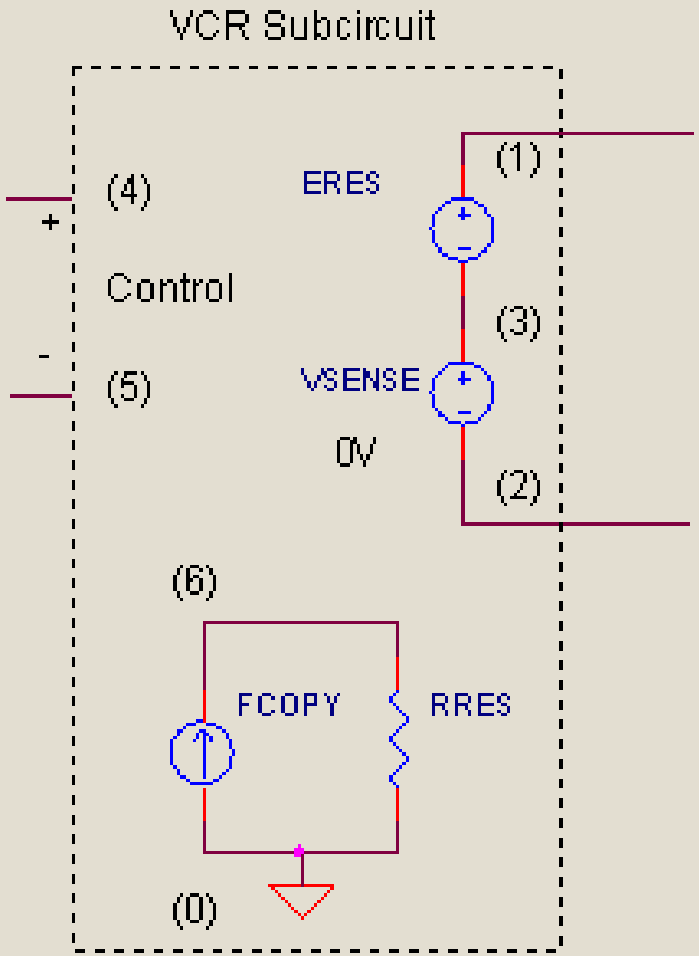
- Shorter Simulation Time
- Reasonably Accurate
- Overestimation of Power Supply Noise

Voltage-Controlled Resistor



- Resistance changes with an applied Control Voltage (V_C)
- Transistors are too complicated

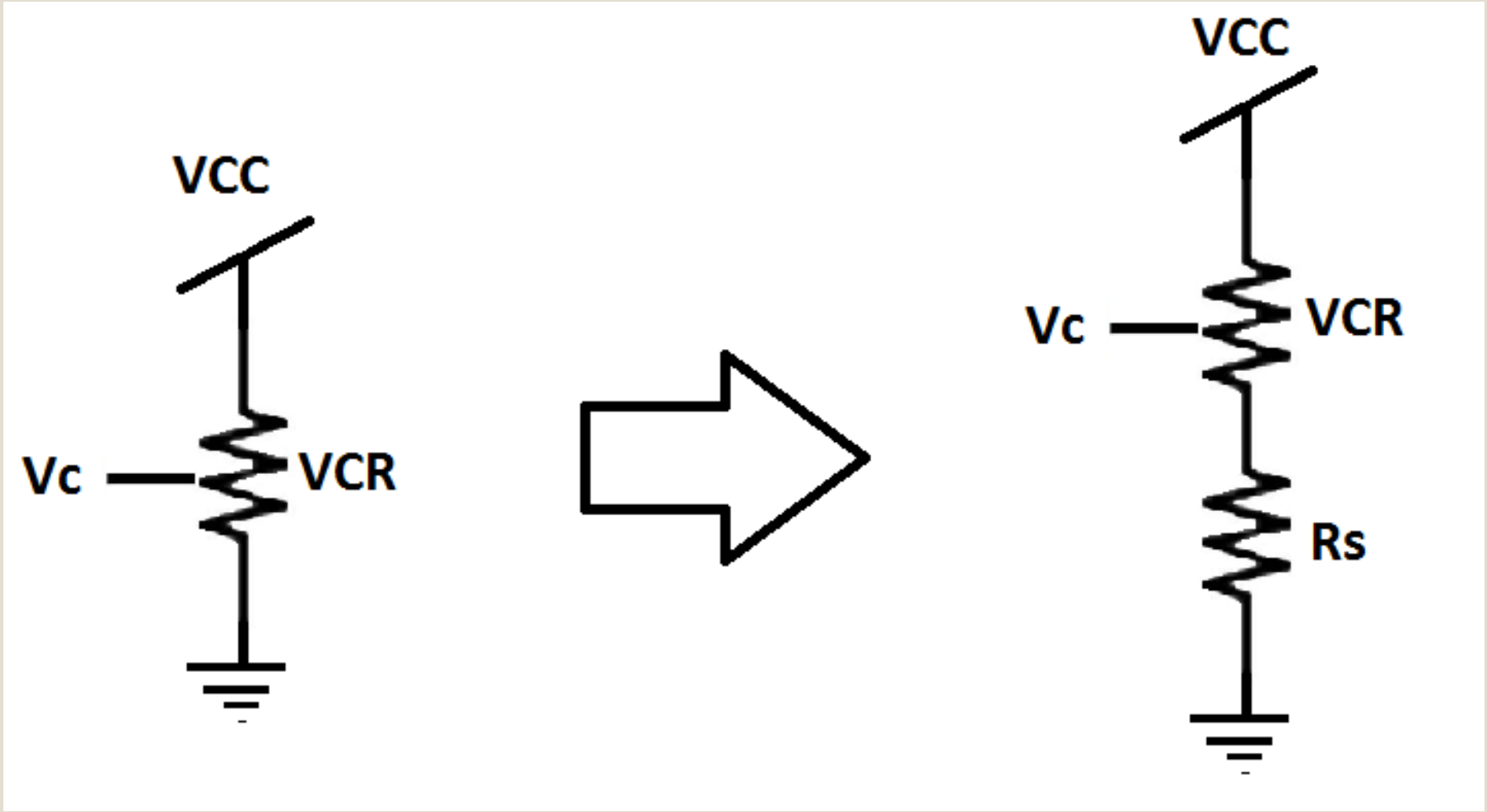
VCR Model



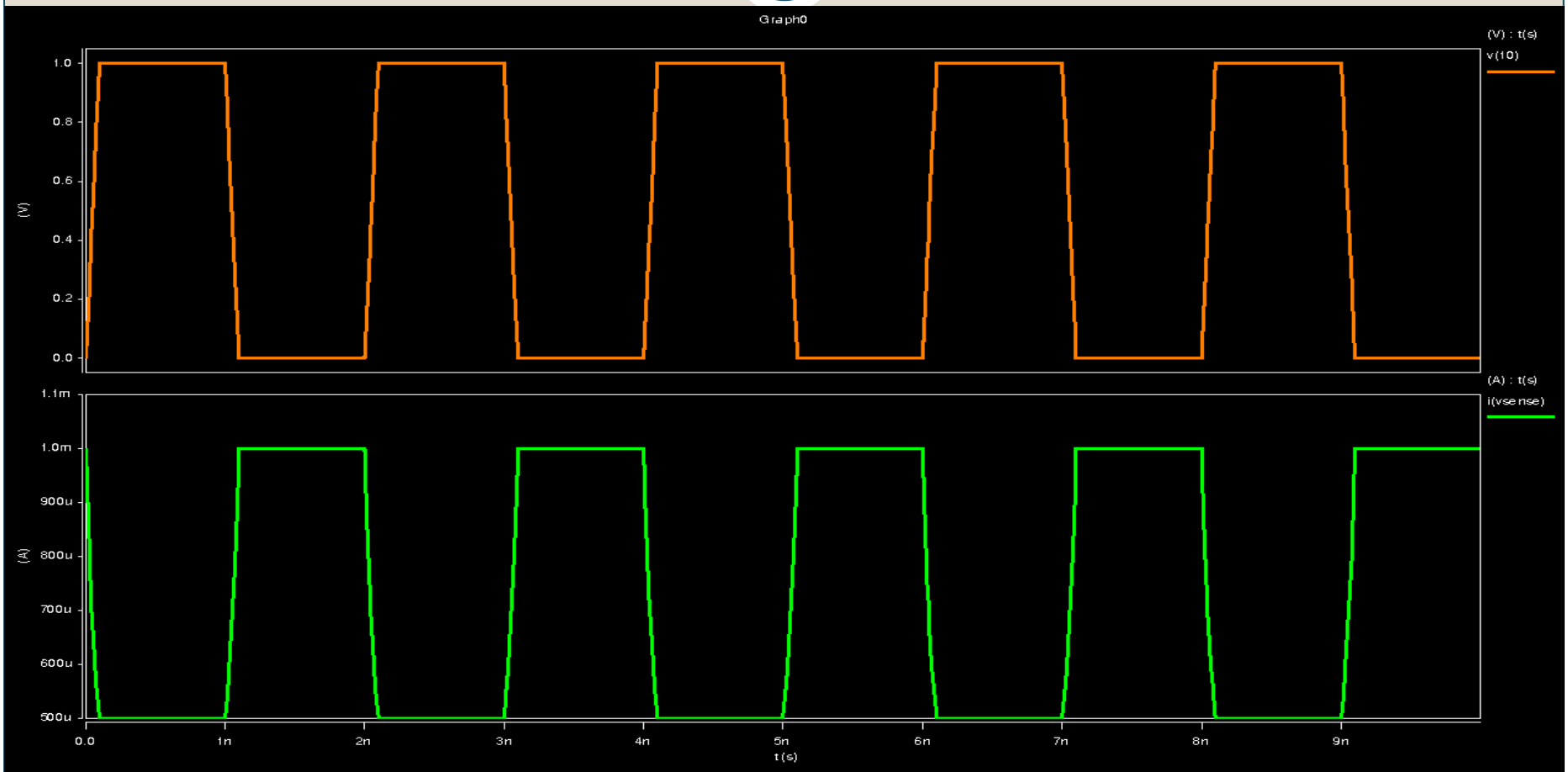
- Voltage-Controlled Voltage Source
- $Vvcr = I \cdot RRES \cdot Vc$

http://www.ecircuitcenter.com/circuits/vc_resistor1/vc_resistor1.htm

Current Generation Circuit



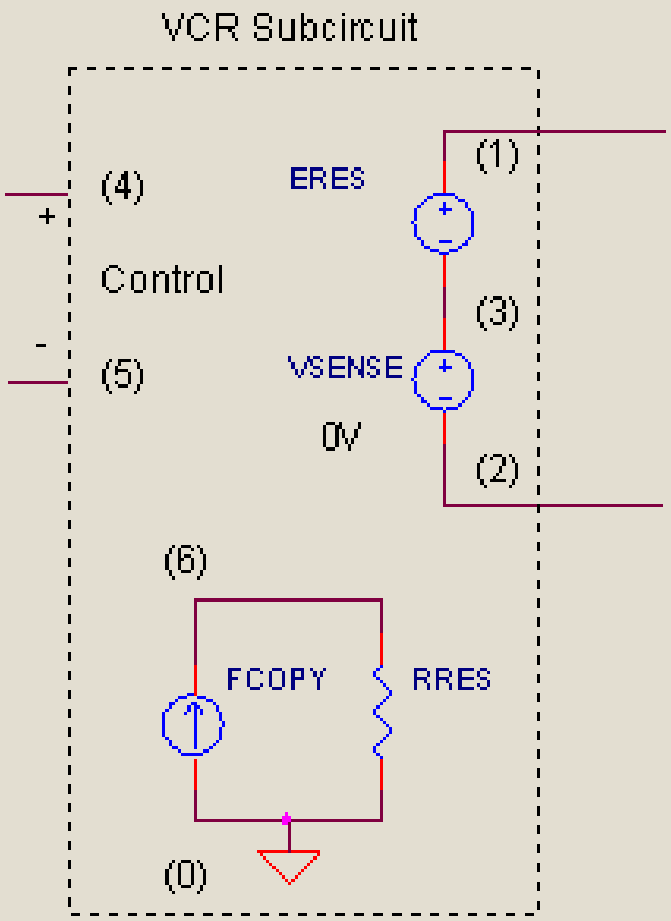
Circuit Test



Orange = Control Voltage

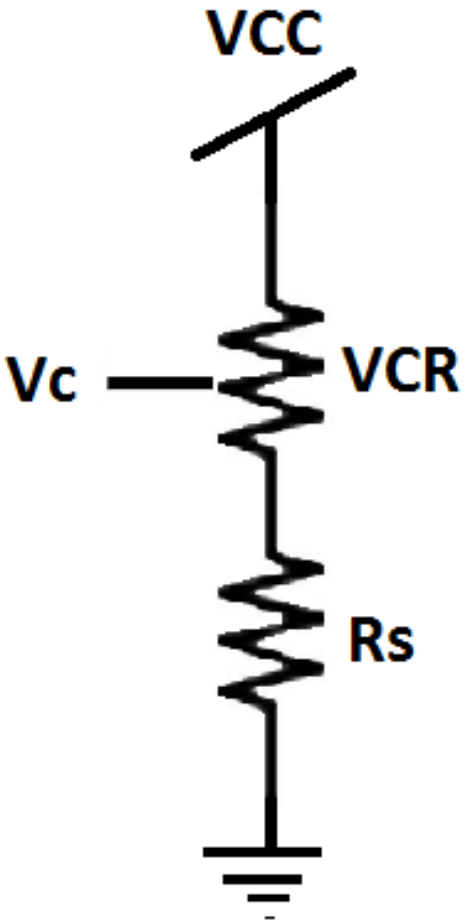
Green = Current

Model Problem



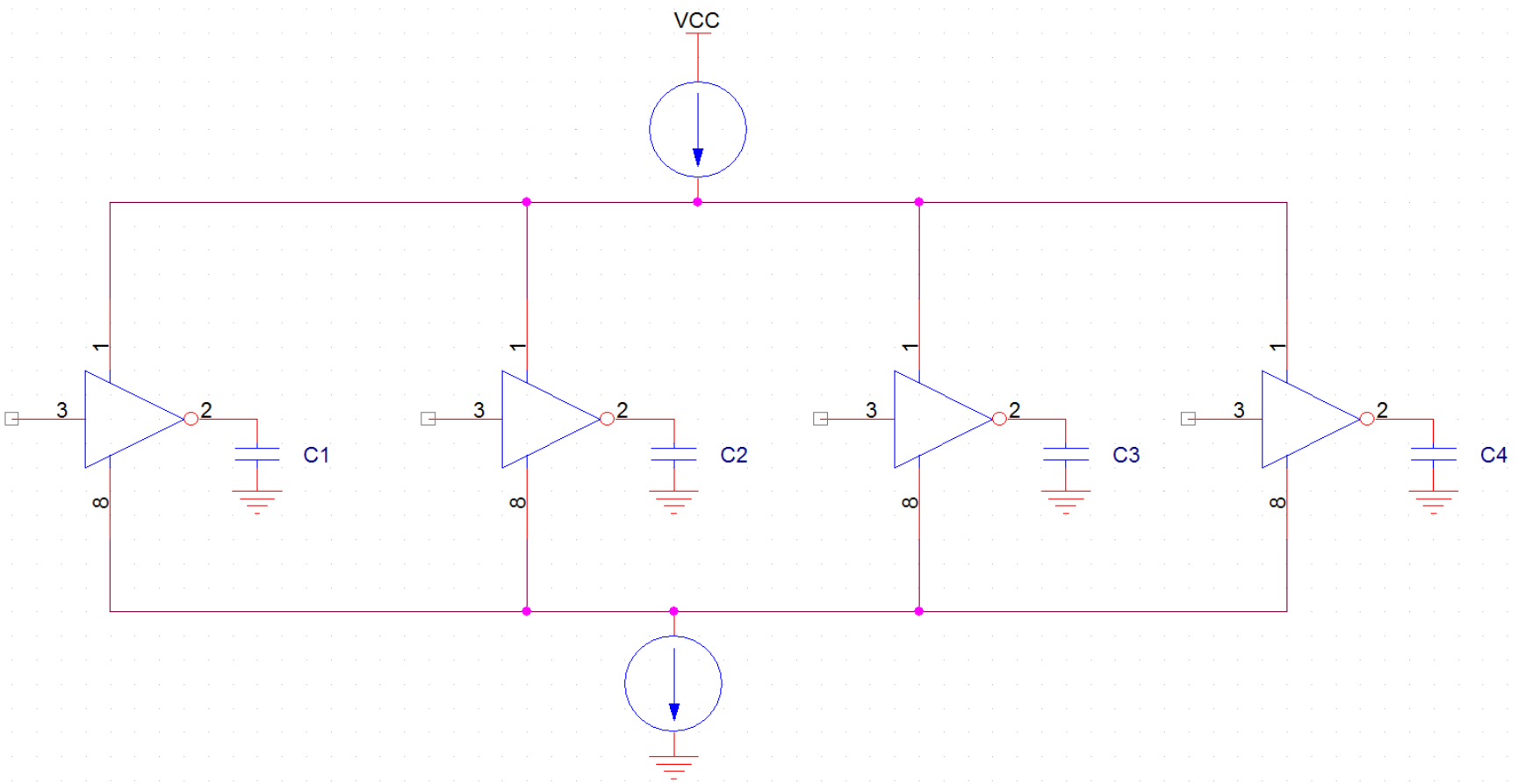
- Dependent Source
  - $Vvcr = \boldsymbol{I} \cdot R \cdot Vc$
- $Vvcr = V \cdot Vc$
- Set FCOPY = 1A
  - RRES = 1Ω
- $Vvcr = 1 \cdot Vc$

Current Translation Equation

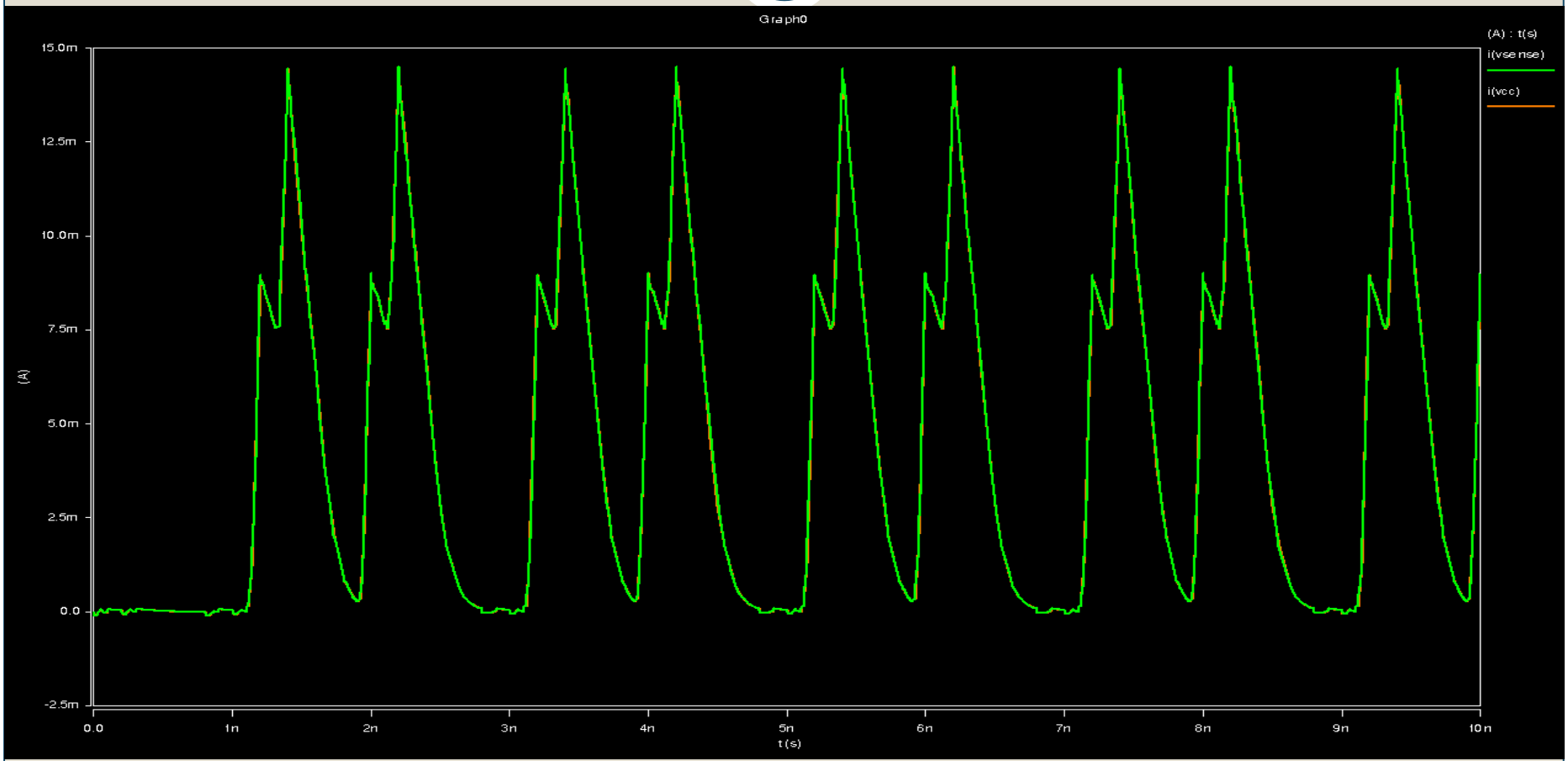


- $I = \frac{Vcc - Vvcr}{Rs}$
  - I = Id
  - Vvcr = Vc
- $Vc = Vcc - (Id \cdot Rs)$

Test 1: Inverter Circuit



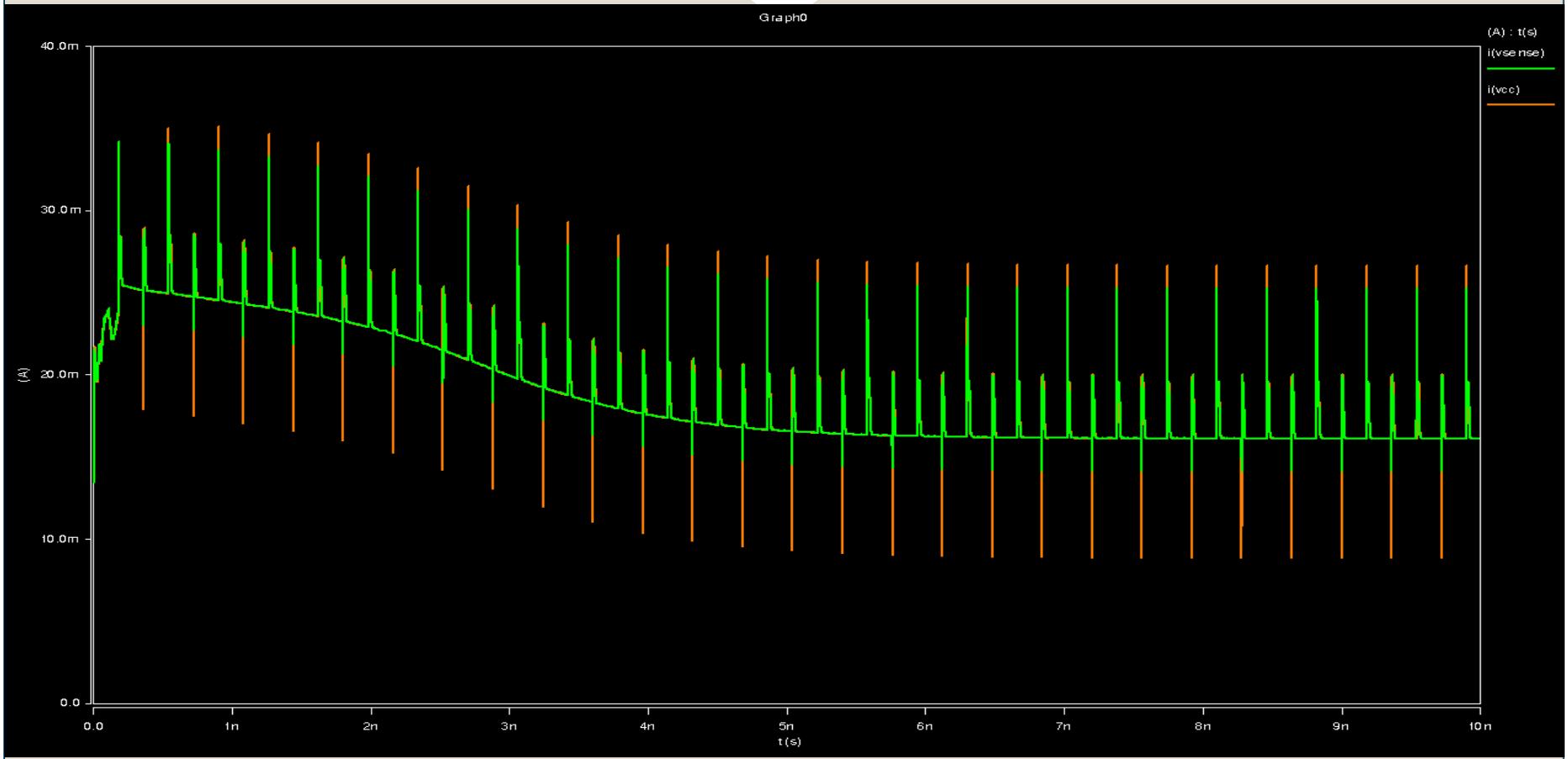
Inverter Icc Waveforms



Orange = Inverter current
Green = VCR current

Max percentage error: 8.5%
Average percentage error: 0.15%

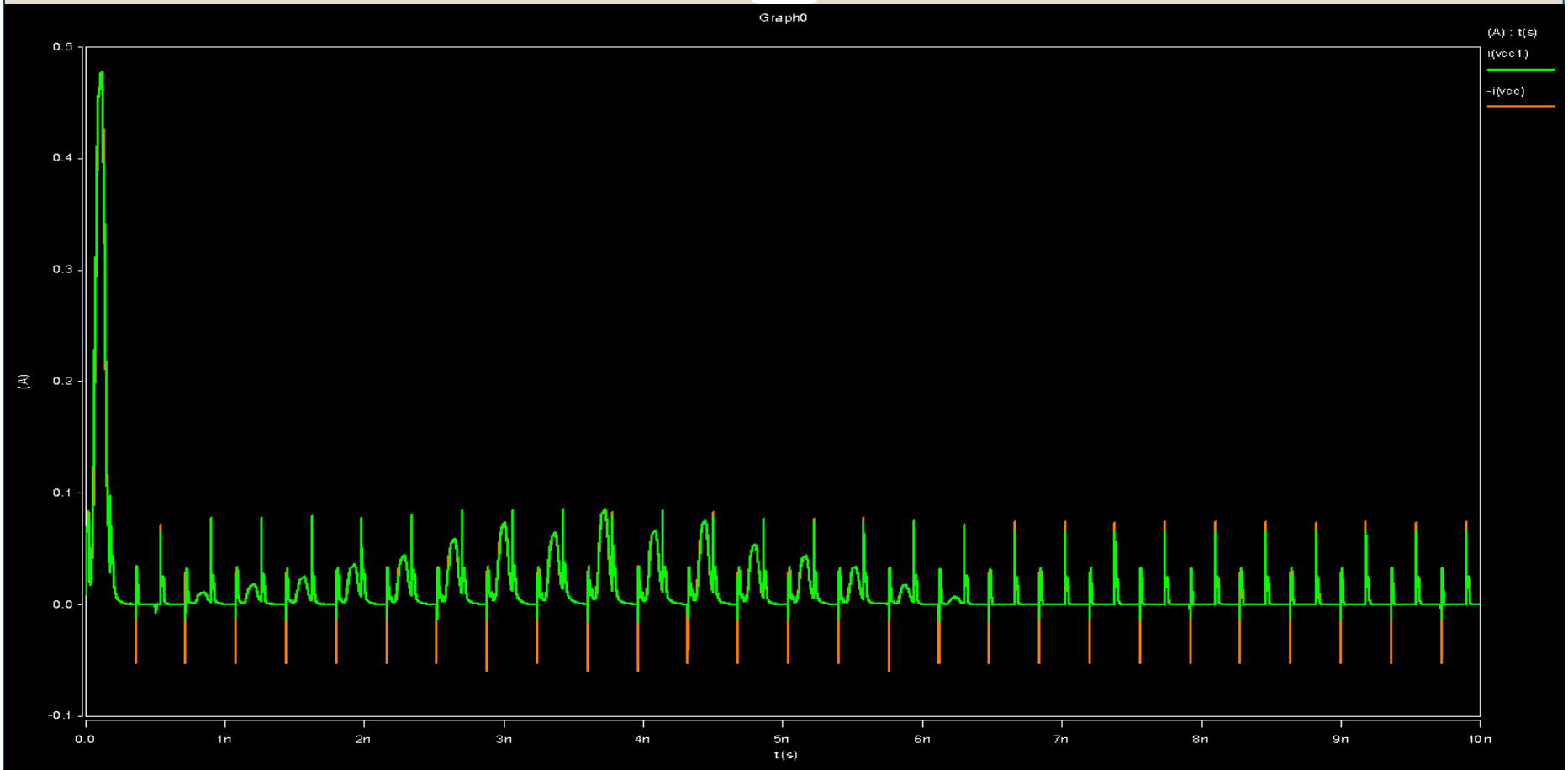
Test 2: 8-bit Multiplier



Orange = Multiplier current
Green = VCR current

Max percentage error: 71%
Average percentage error: 0.18%

Test 3: Fibonacci 16



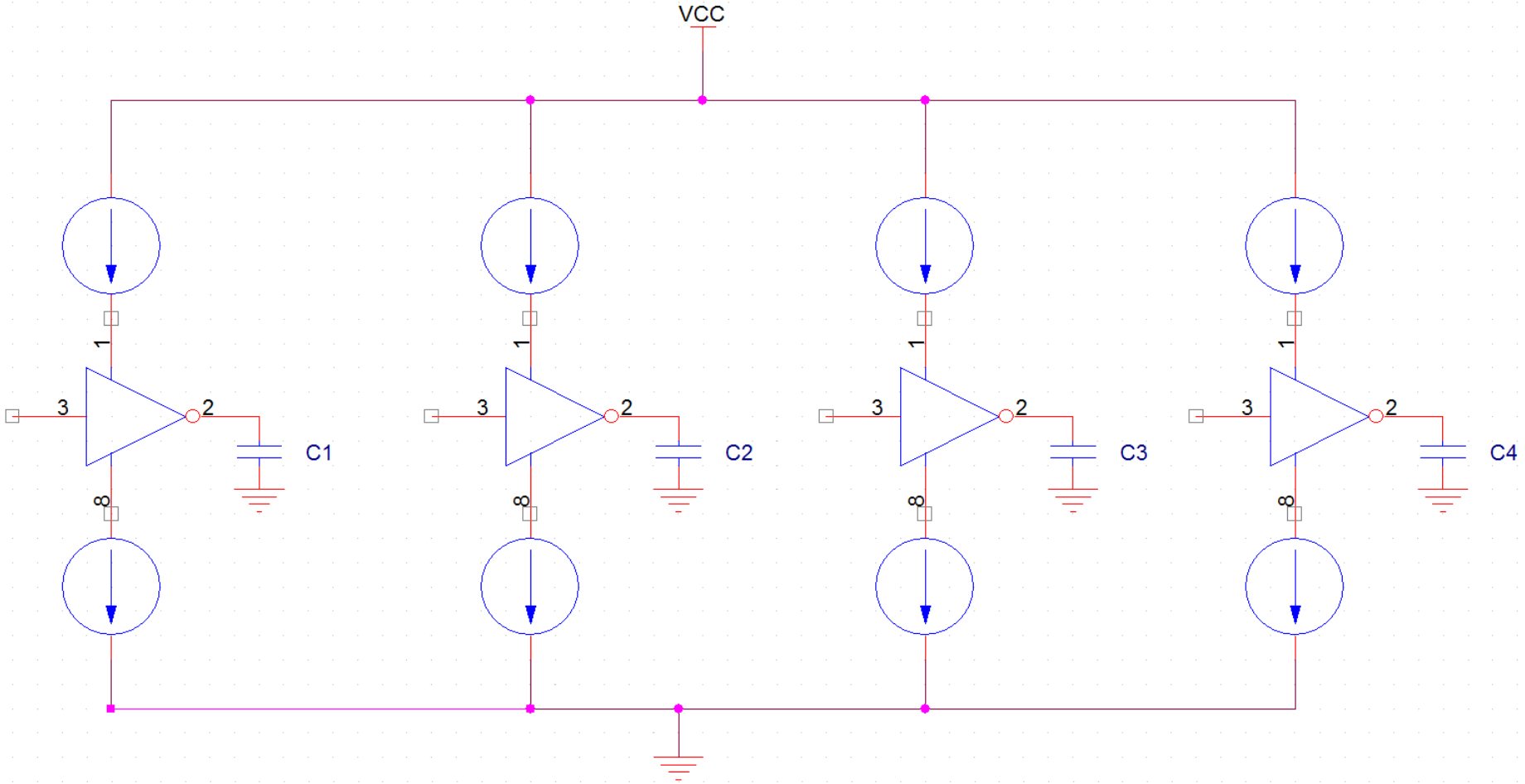
Orange = Fibonacci current

Green = VCR current

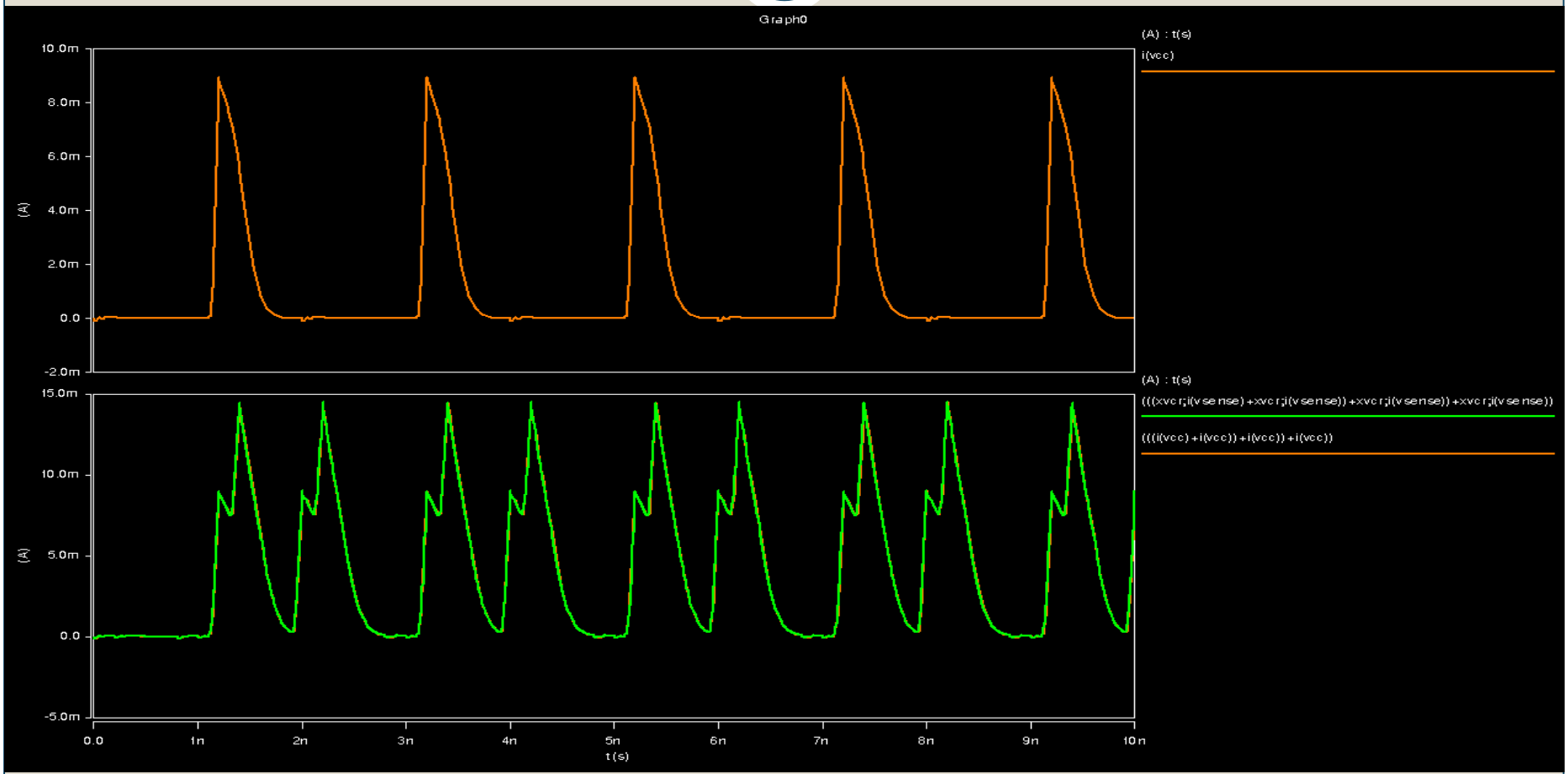
Max percentage error: 285%

Average percentage error: 1.2%

Inverter test 2



Inverter Test 2 Results



Orange = Inverter current

Green = VCR current

Max percentage error: 5.5%

Average percentage error: 0.14%

Timing Comparison

Circuit Simulated	Circuit		VCR		Current Source	
	CPU Time	Total Time	CPU Time	Total Time	CPU Time	Total Time
Inverter	.76 s	1.08 s	.07 s	.273 s	.07 s	.256 s
16-bit Adder	7.97 s	8.31 s	.08 s	.347 s	.08 s	.273 s
16-bit Multiplier	27.8 s	28.89 s	.137 s	.44 s	.08 s	.327 s
Fibonacci 4	40.64 s	41.69 s	.107 s	.353 s	.077 s	.293 s
Fibonacci 8	91.6 s	95.46 s	.1 s	.363 s	.08 s	.305 s
Fibonacci 16	229.5 s	231.7 s	.12 s	.393 s	.08 s	.313 s

Conclusion

- Replace current source with VCR
- Designed Current Generation Circuit
- VCR accurate for simple waveforms
- Further experimentation is required

Questions?

Contact Information:

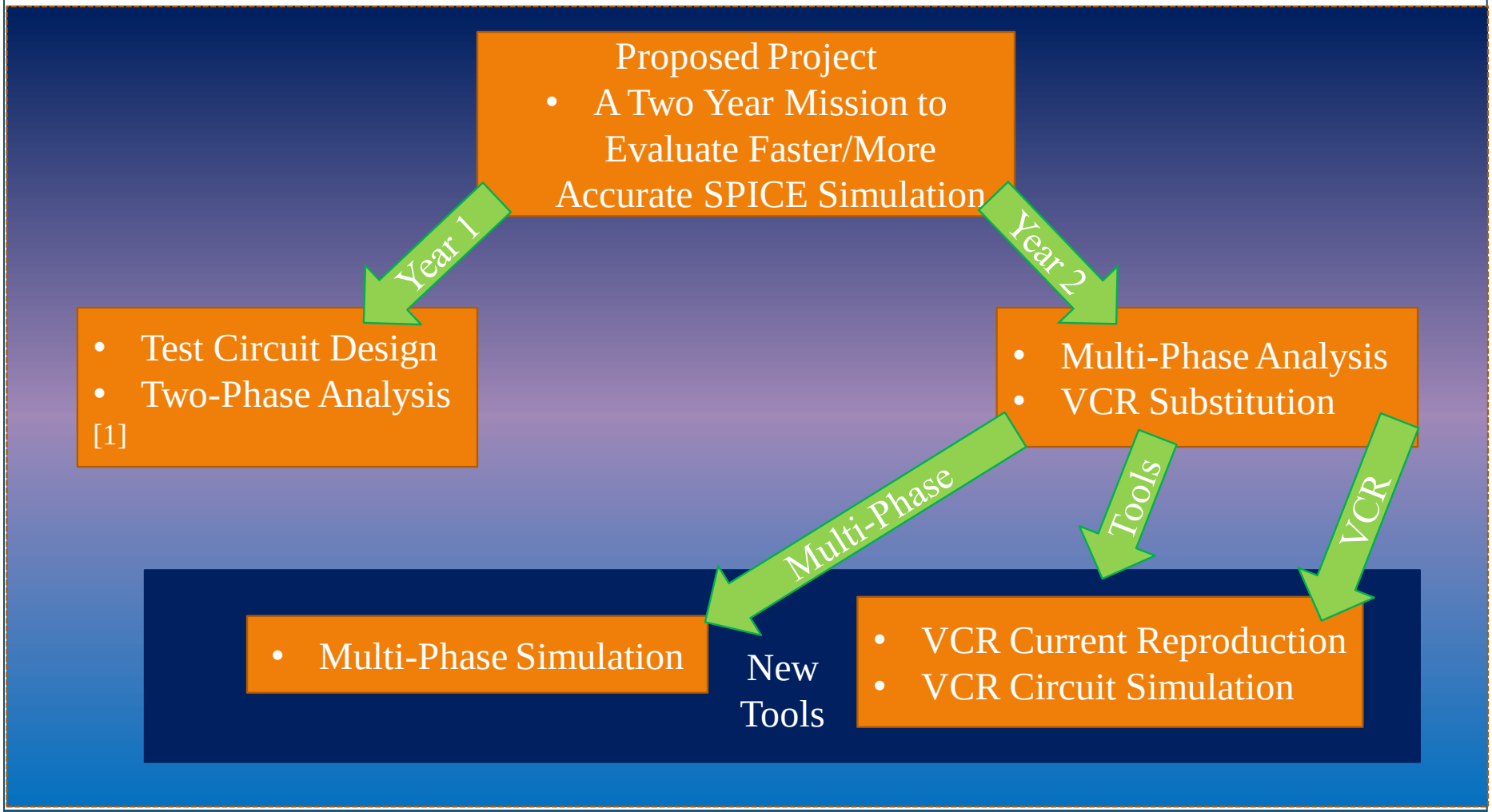
Travis.Fiehler@utah.edu

References:

[1] T. Hollis, “University of Utah Senior Clinic 2010-2011,” Micron Technology, Boise, Idaho, 2010.

[2] “Voltage-Controlled Resistor,” http://www.ecircuitcenter.com/circuits/vc_resistor1/vc_resistor1.htm. Accessed: 3/28/2011

Alternate Two Phase Model Using VCR Measurements and Analysis



Overview

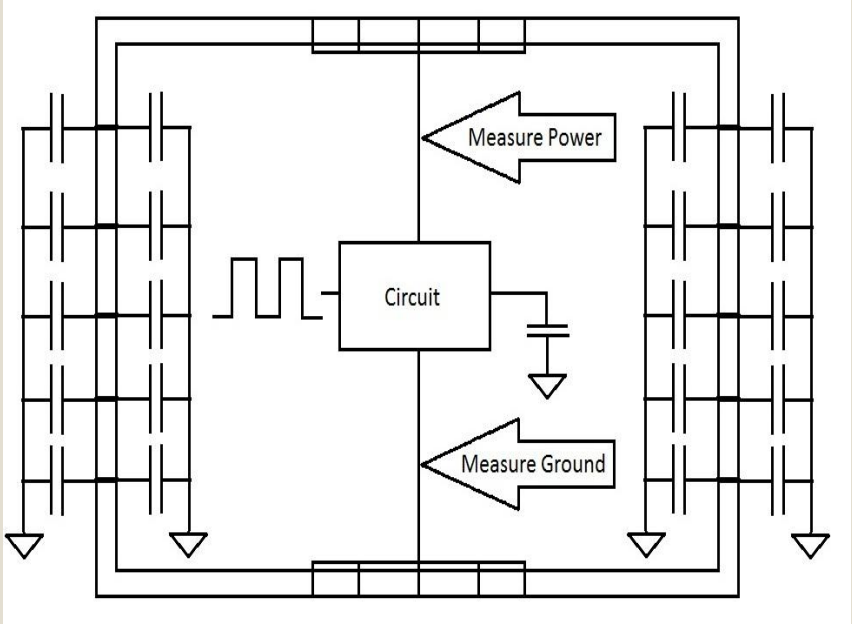
- Alternate Two-Phase VCR Method
- Simulation Flow
- Initial Configuration
  - Sensitivity of Varying Resistance And Capacitance
  - Results
- Revised Configuration
  - Results
- Practical Configuration
  - Results
- Comparison with Multi-Phase Results
- Simulations Runtimes
- Future Considerations
- Conclusion

Two-Phase VCR Introduction

- Use the VCR in Two-Phase Method
- Compare with HSPICE
  - Simulation Runtimes
  - Accuracy
- Circuits created by last year's Micron Team: [1]
  - Four-Inverter
  - 16-Bit Adder
  - 8-Bit Multiplier
  - 4-Stage Fibonacci
  - 8-Stage Fibonacci
  - 16-Stage Fibonacci

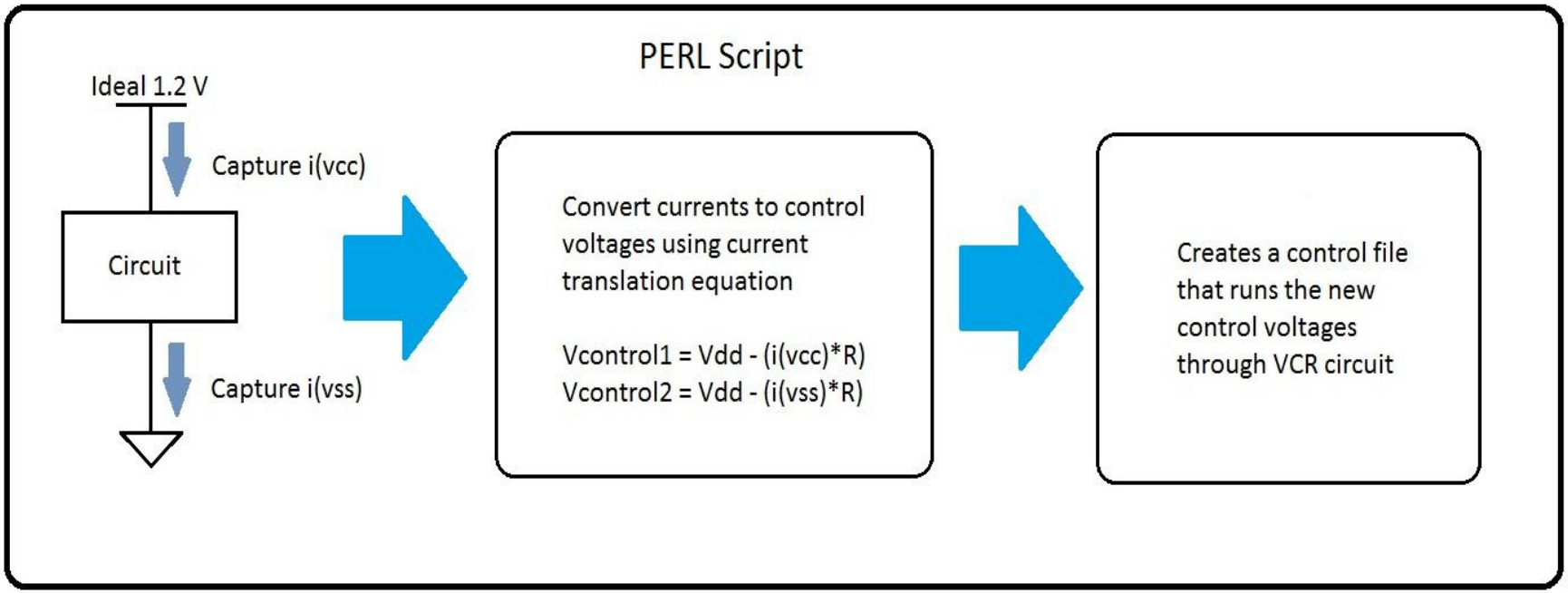
Baseline HSPICE Simulation

- Provides the standard for comparisons
- Reduce mutual inductance by placing capacitors at all pins excluding power and ground pins

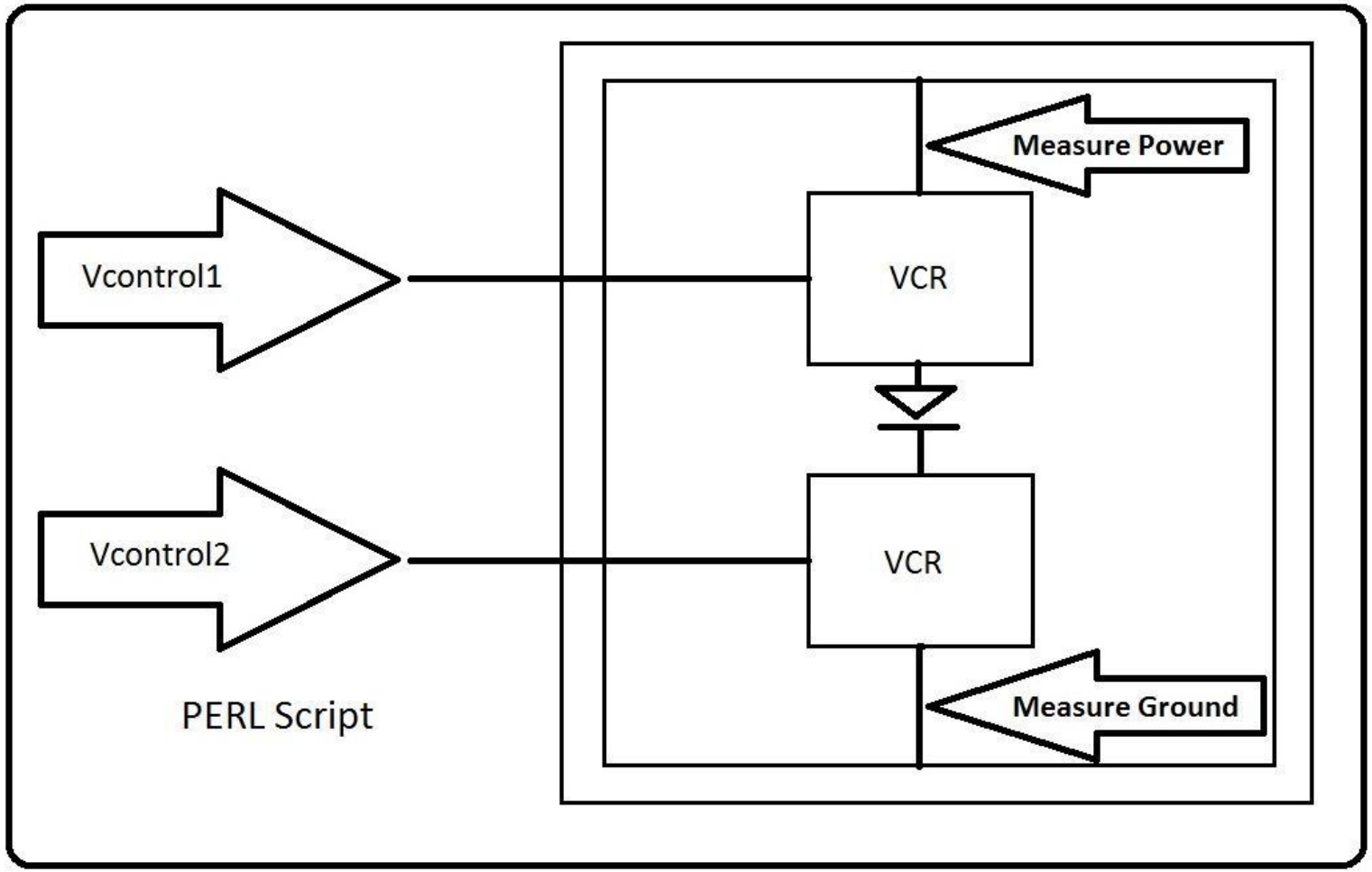


[2]

VCR Two-Phase Simulation Flow

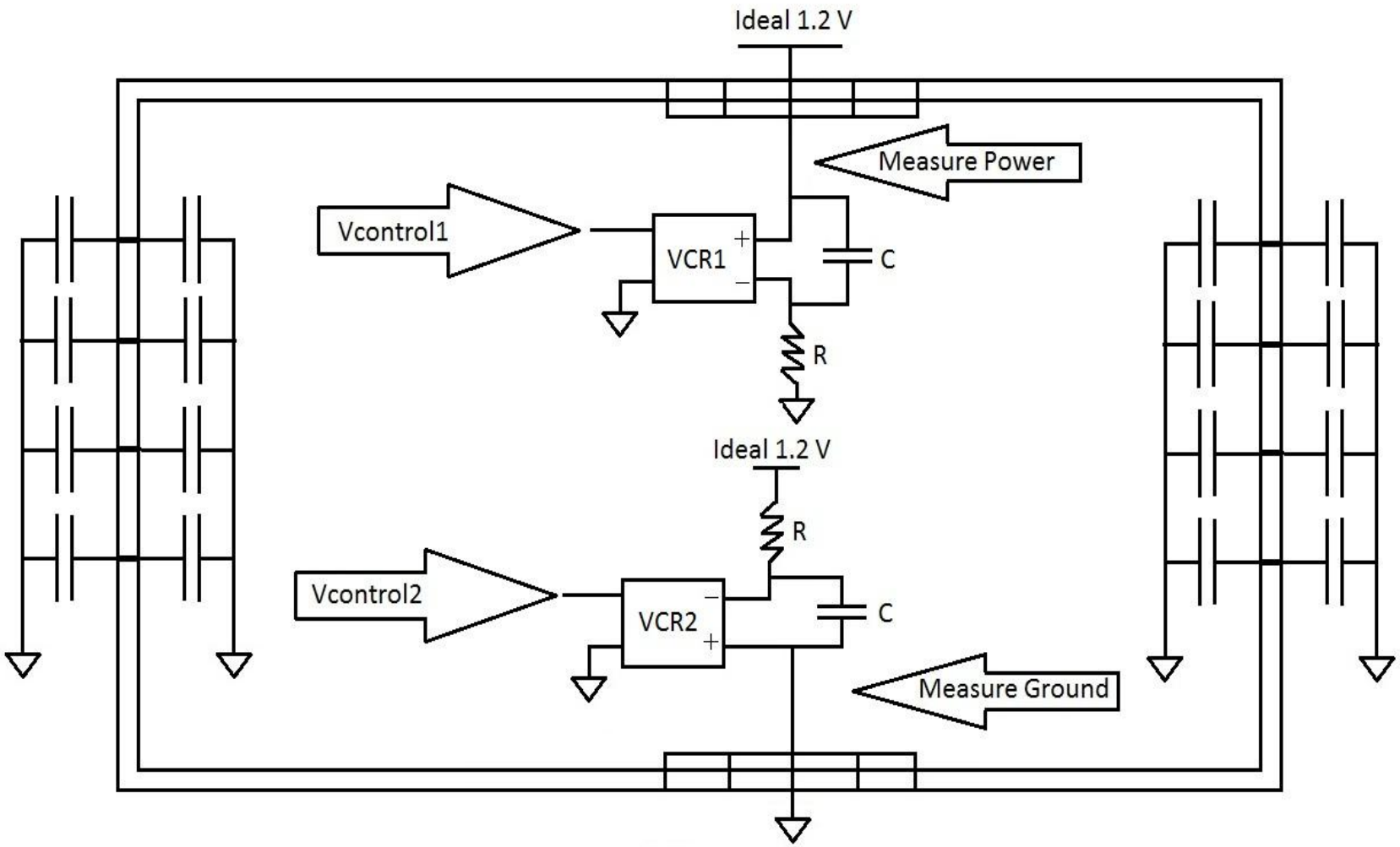


VCR Two-Phase Simulation Flow Continued

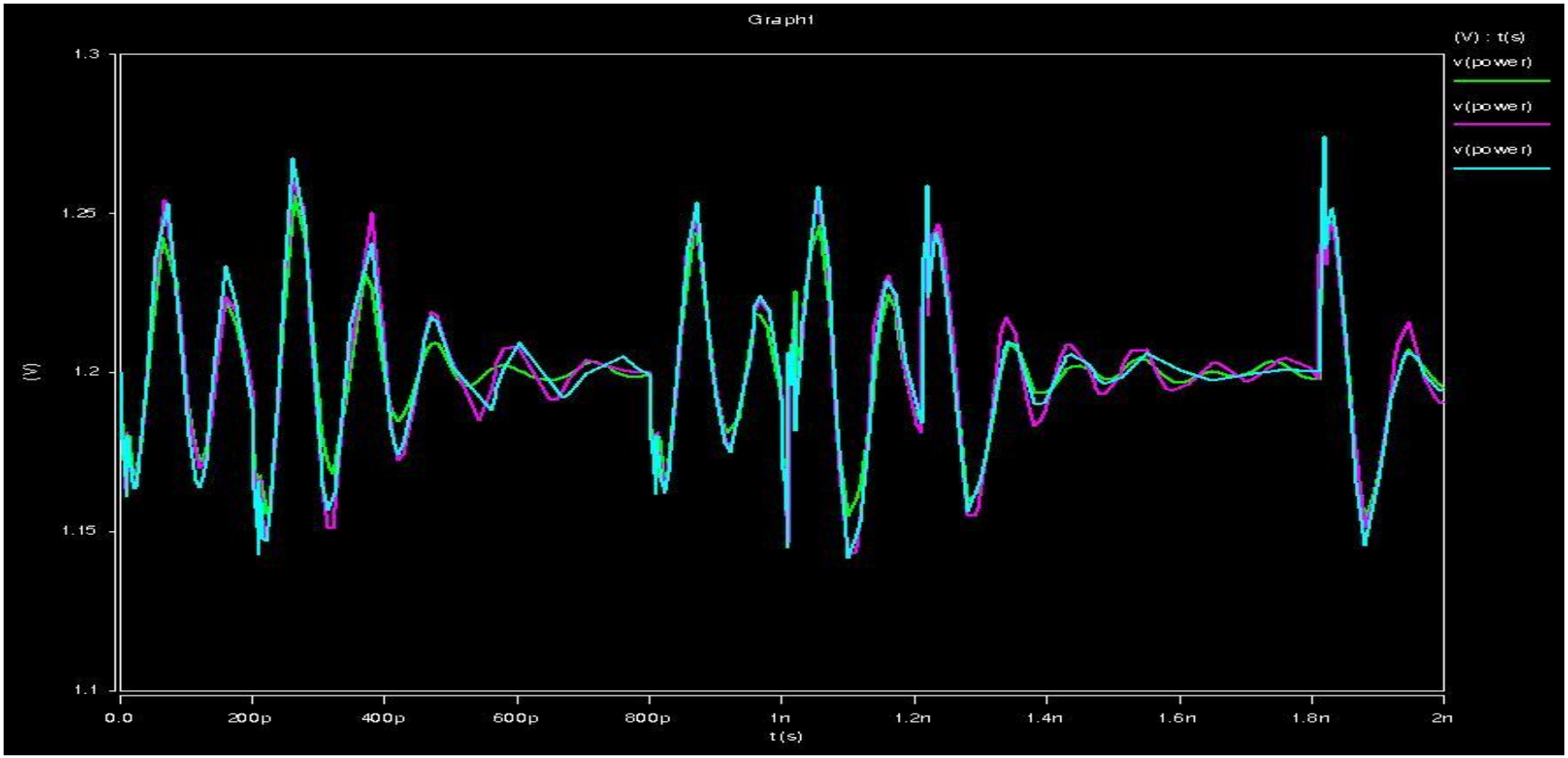


[3]

Initial Configuration

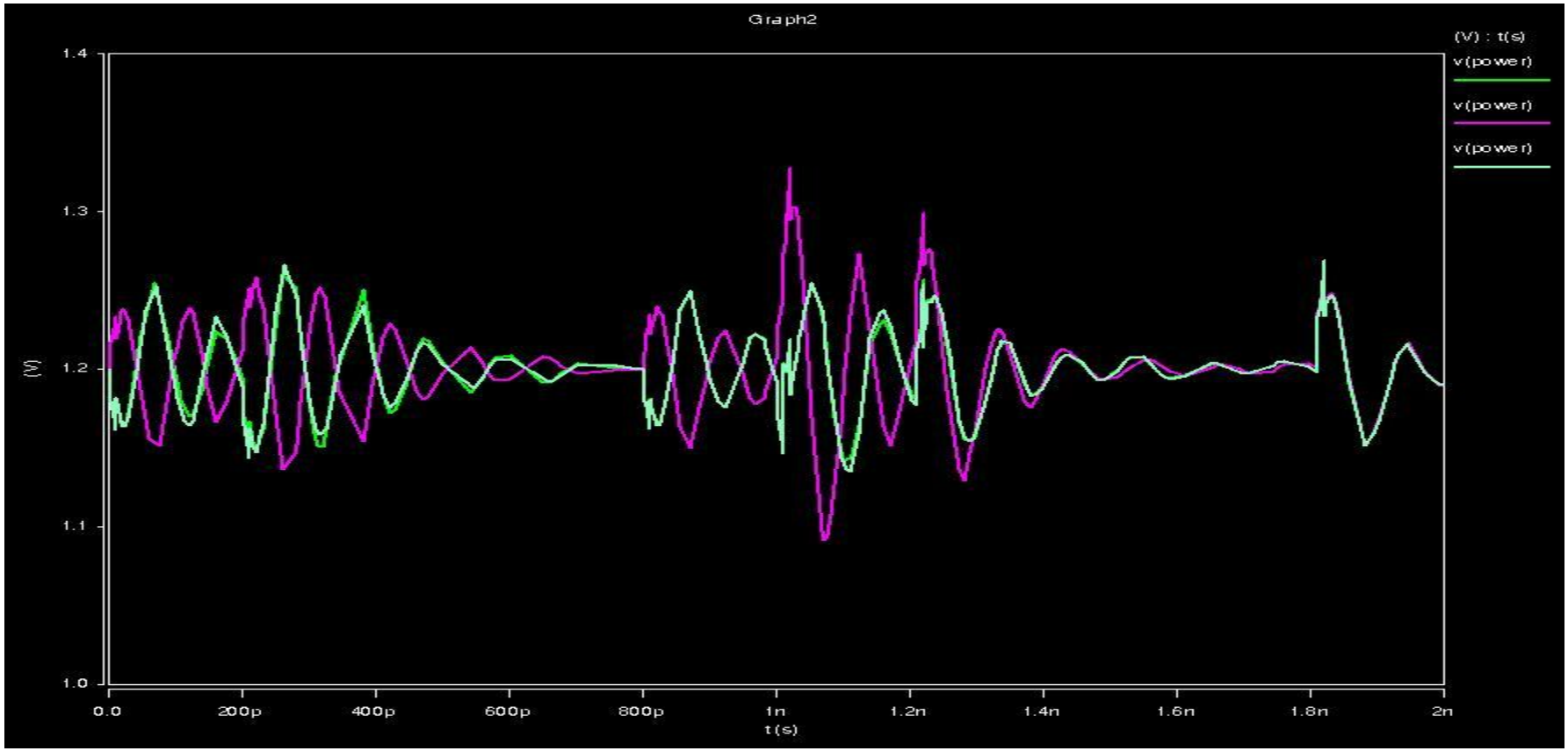


Sensitivity to Varying Resistance



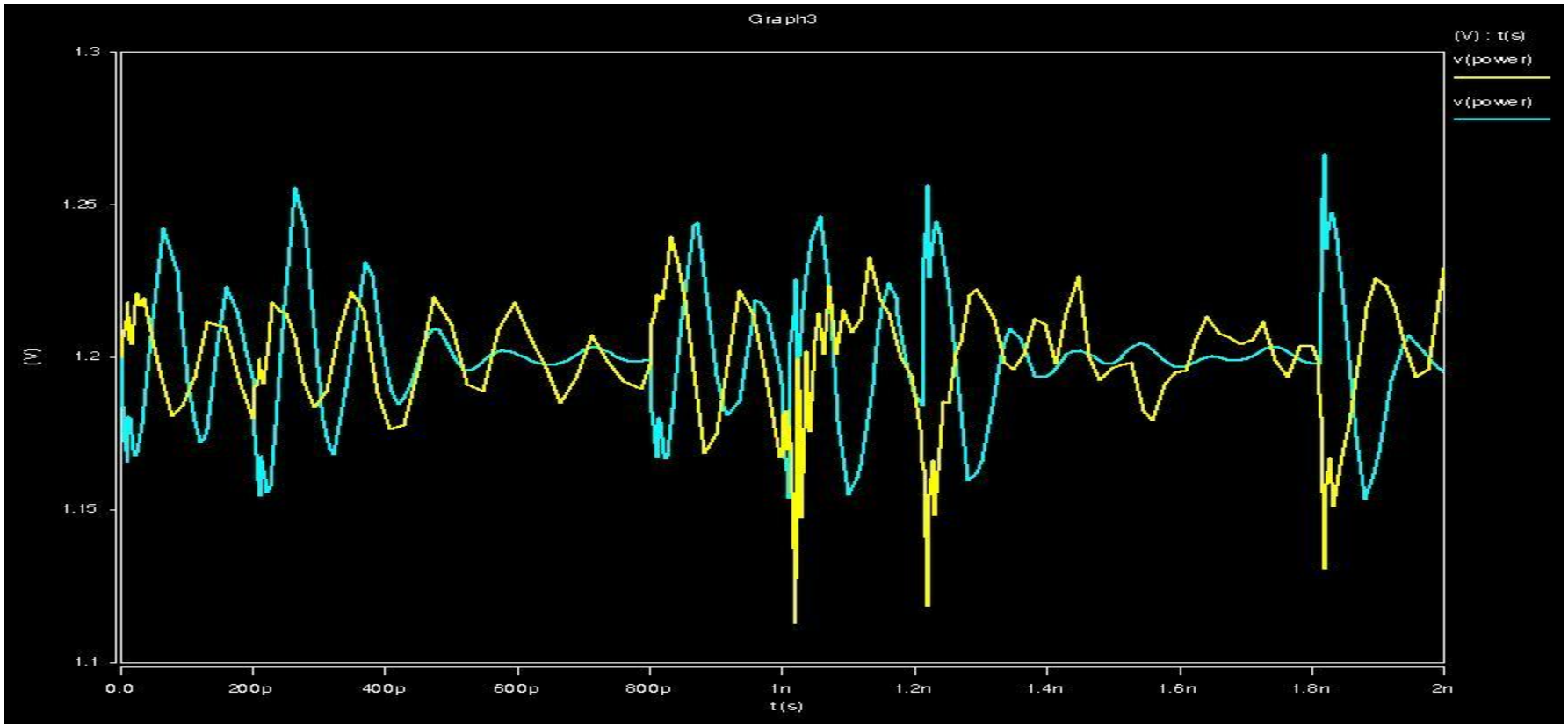
Green- 100 ohms Purple- 1k ohms Blue-3k ohms

Sensitivity to Varying Capacitance



Green- 1fF Purple- 100 pF Pink- 1 mF

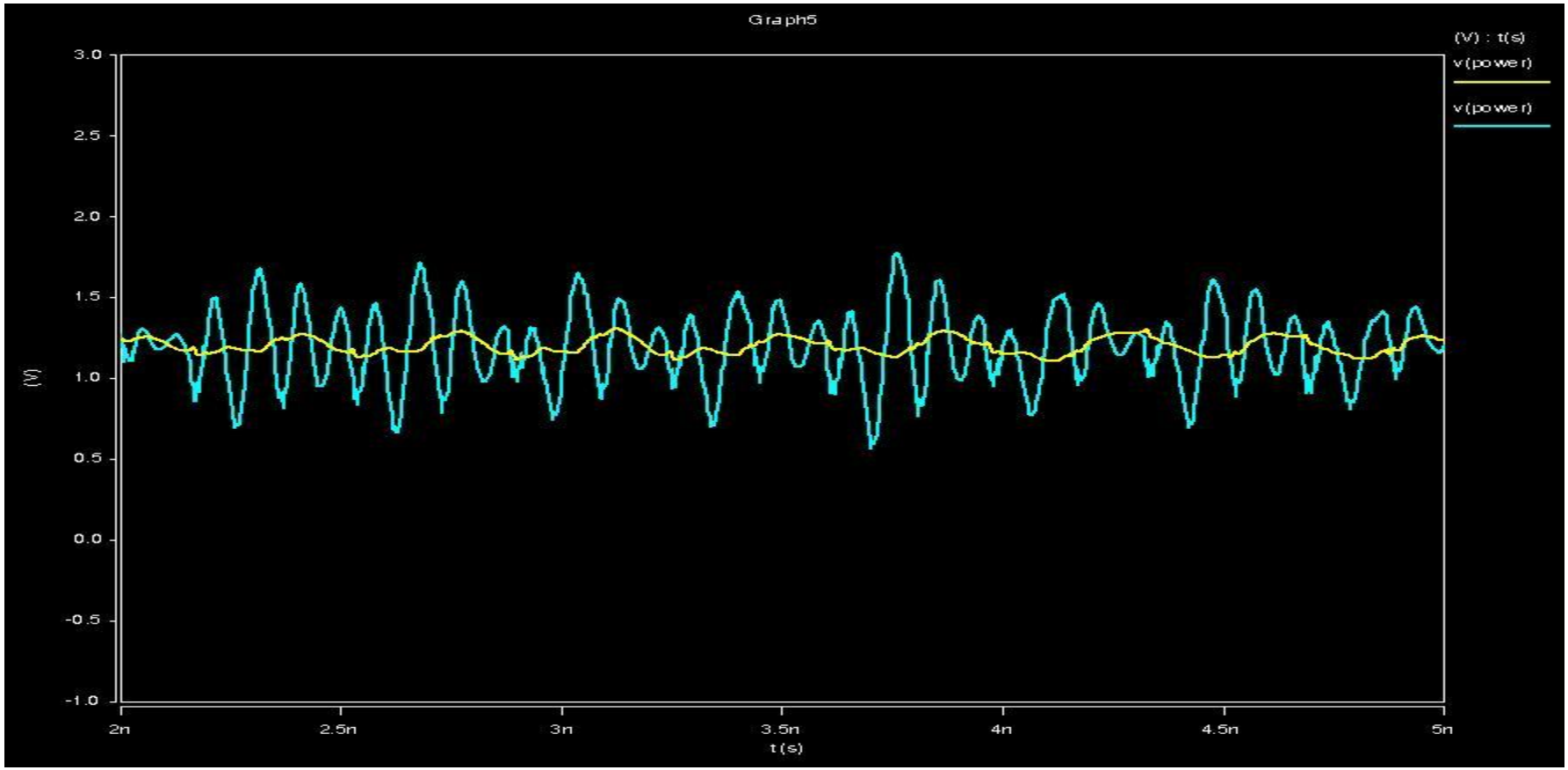
Inverter Results



Yellow- HSPICE Simulation

Blue- Inverter Simulation

16-Stage Fibonacci Results



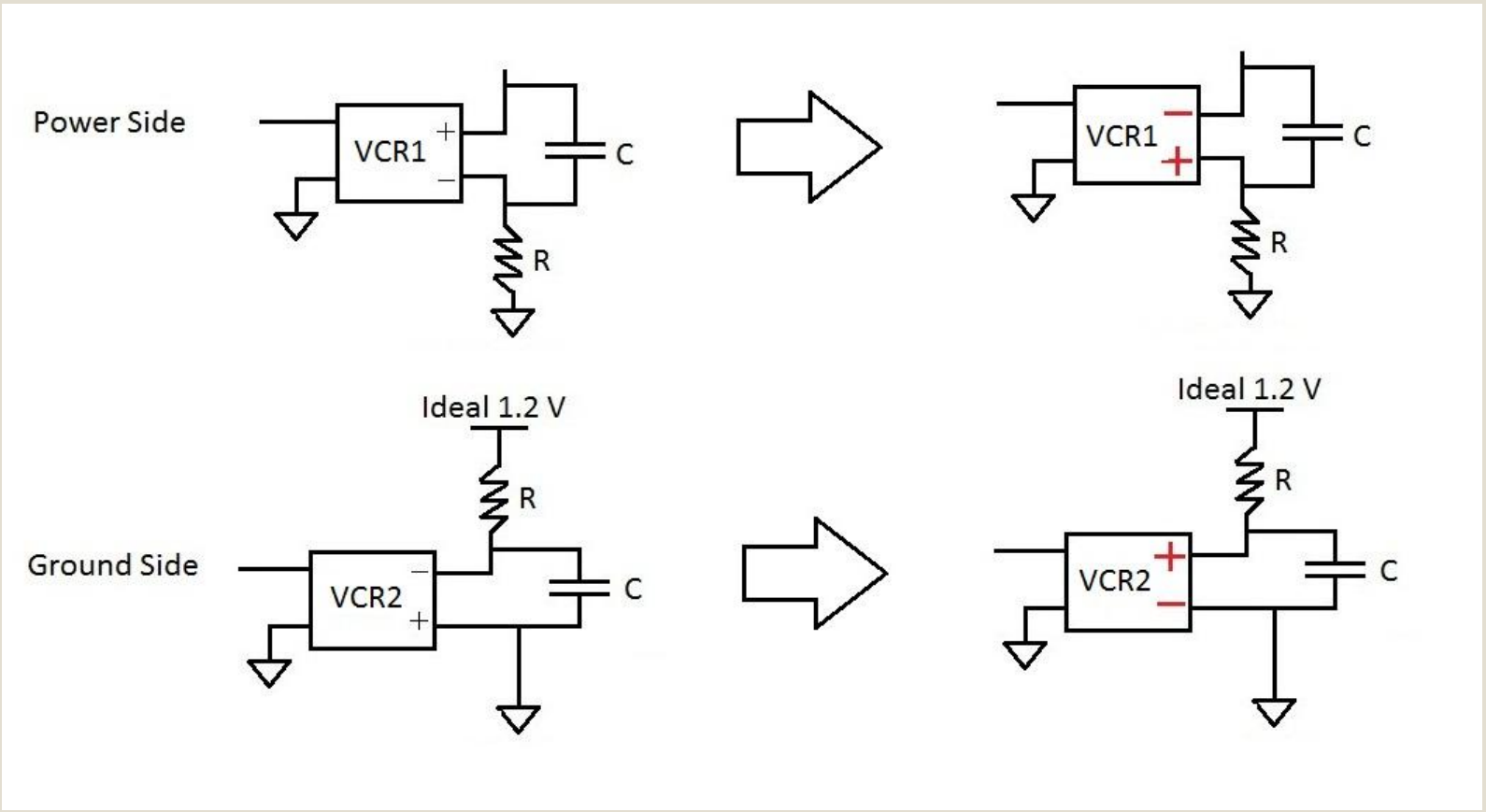
Yellow- Baseline HSPICE Simulation Green – 16 Stage Fibonacci Simulation

Problems with Initial Setup

- Power and Ground Rails are too messy
- No single capacitor value to correctly model circuit's capacitance
- Most circuits modeled required modification to VCRs

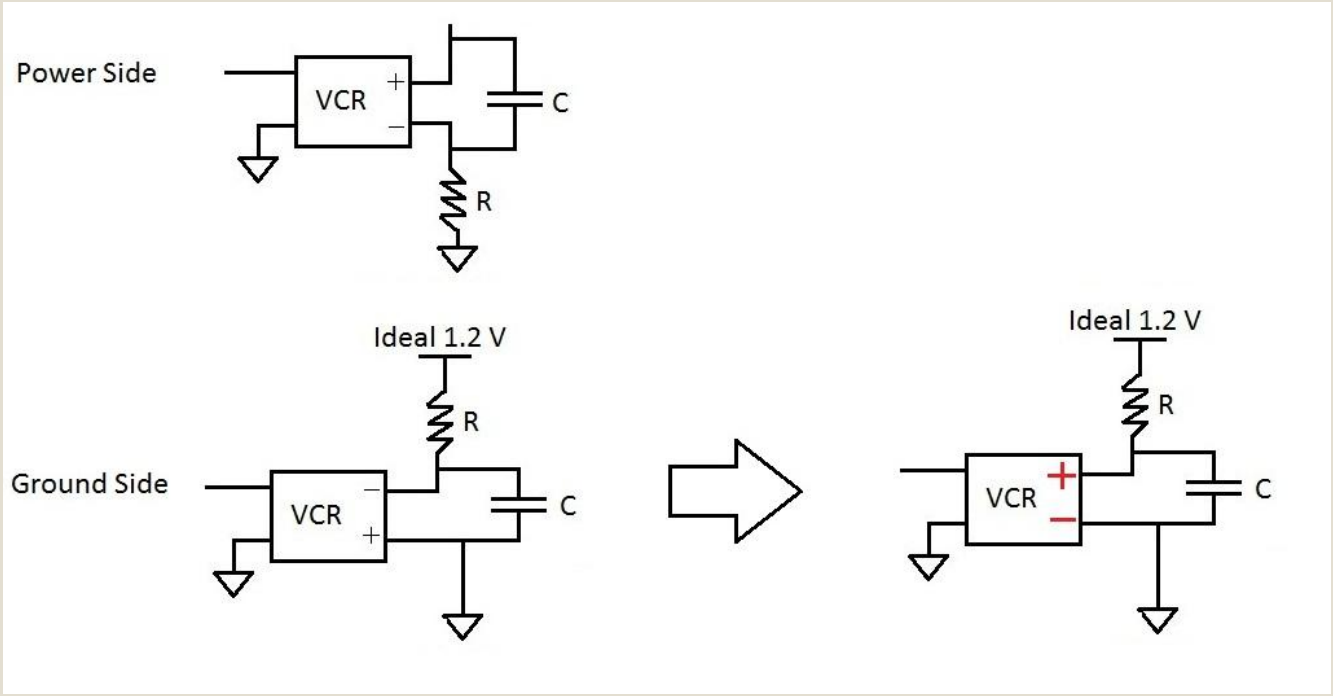
Inverter Modifications

- Both polarities of VCR1 and VCR2 are swapped

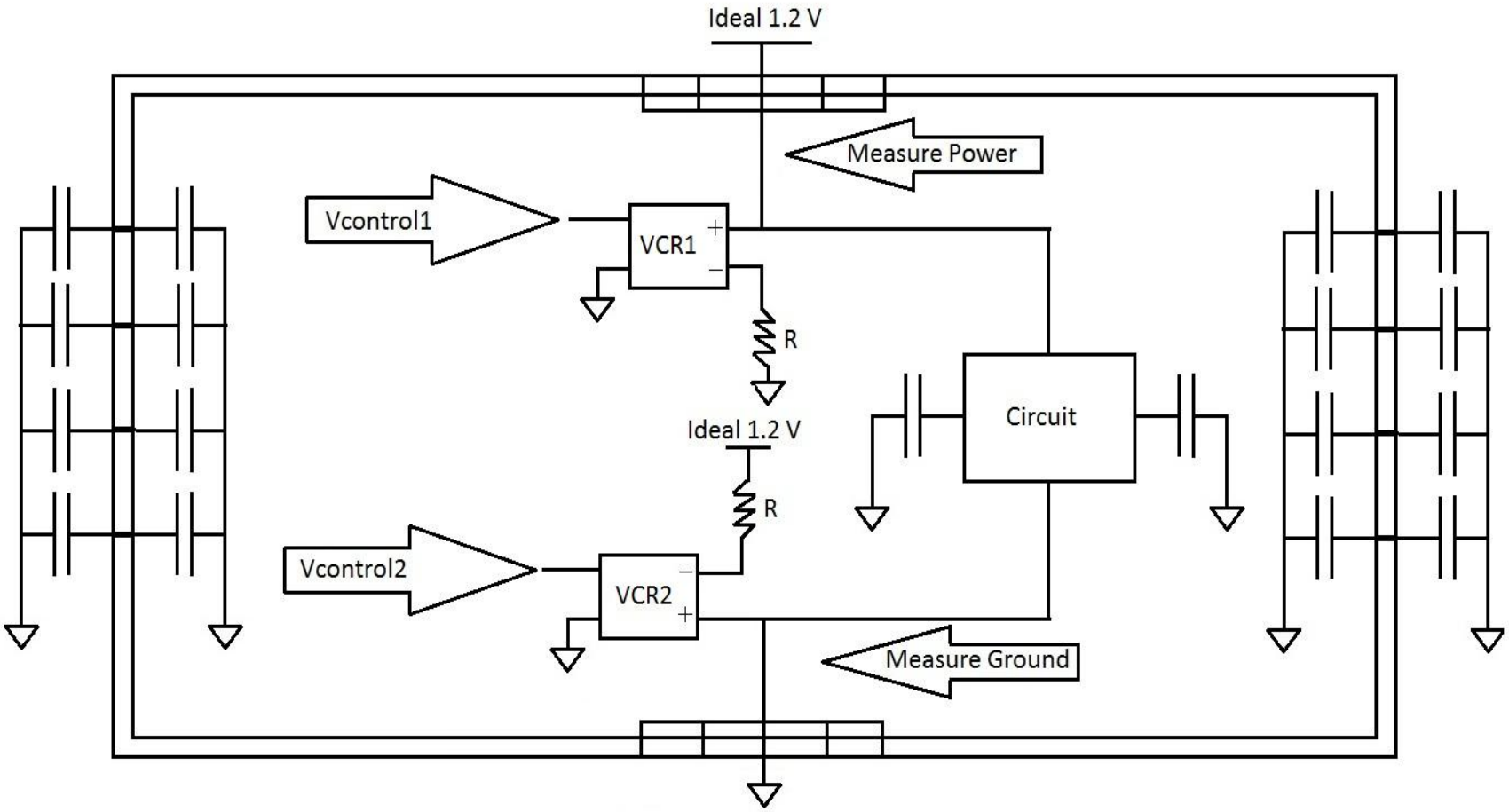


Adder & Fibonacci Modifications

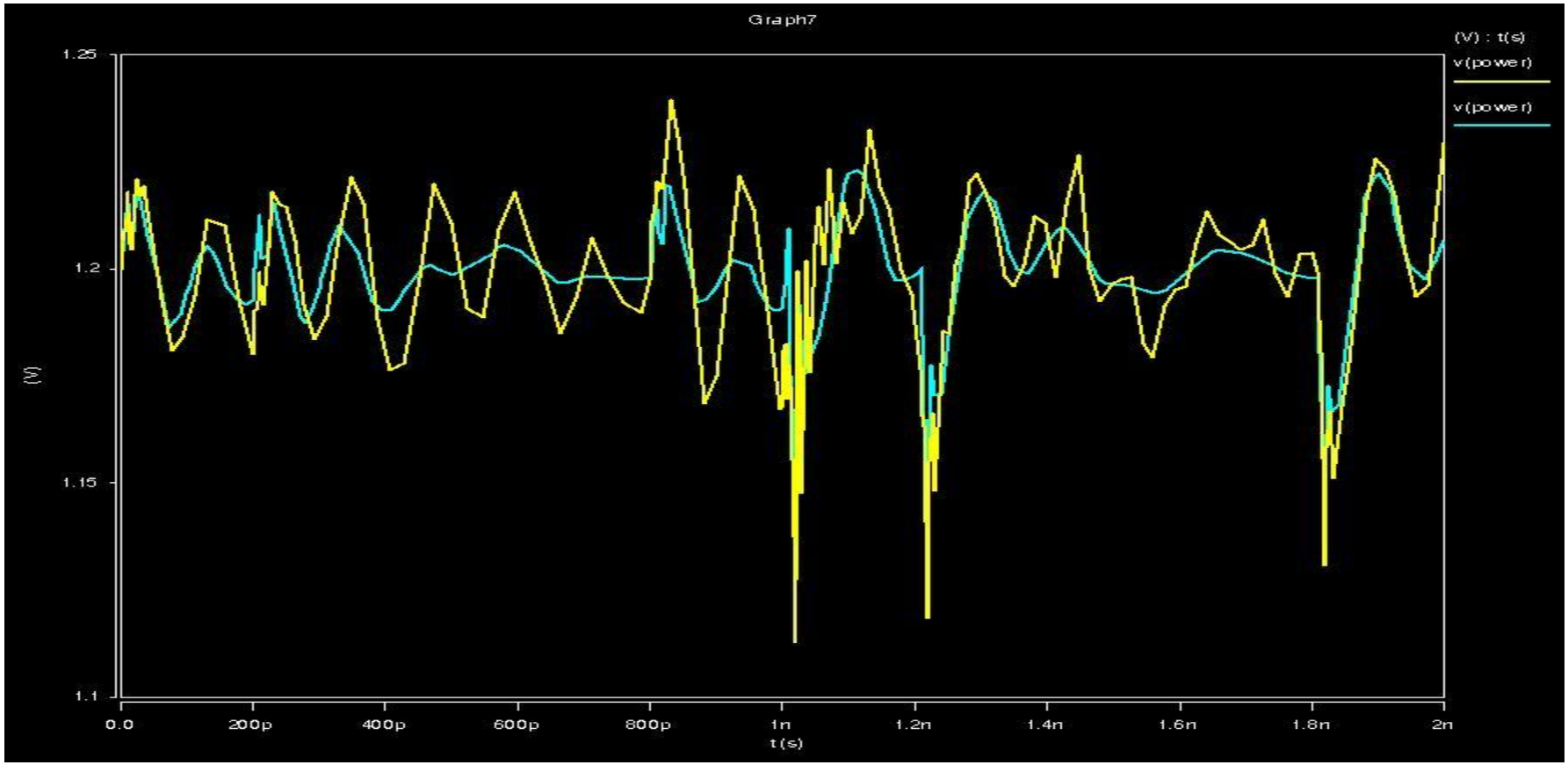
- Polarity of VCR2 is swapped



Revised Configuration

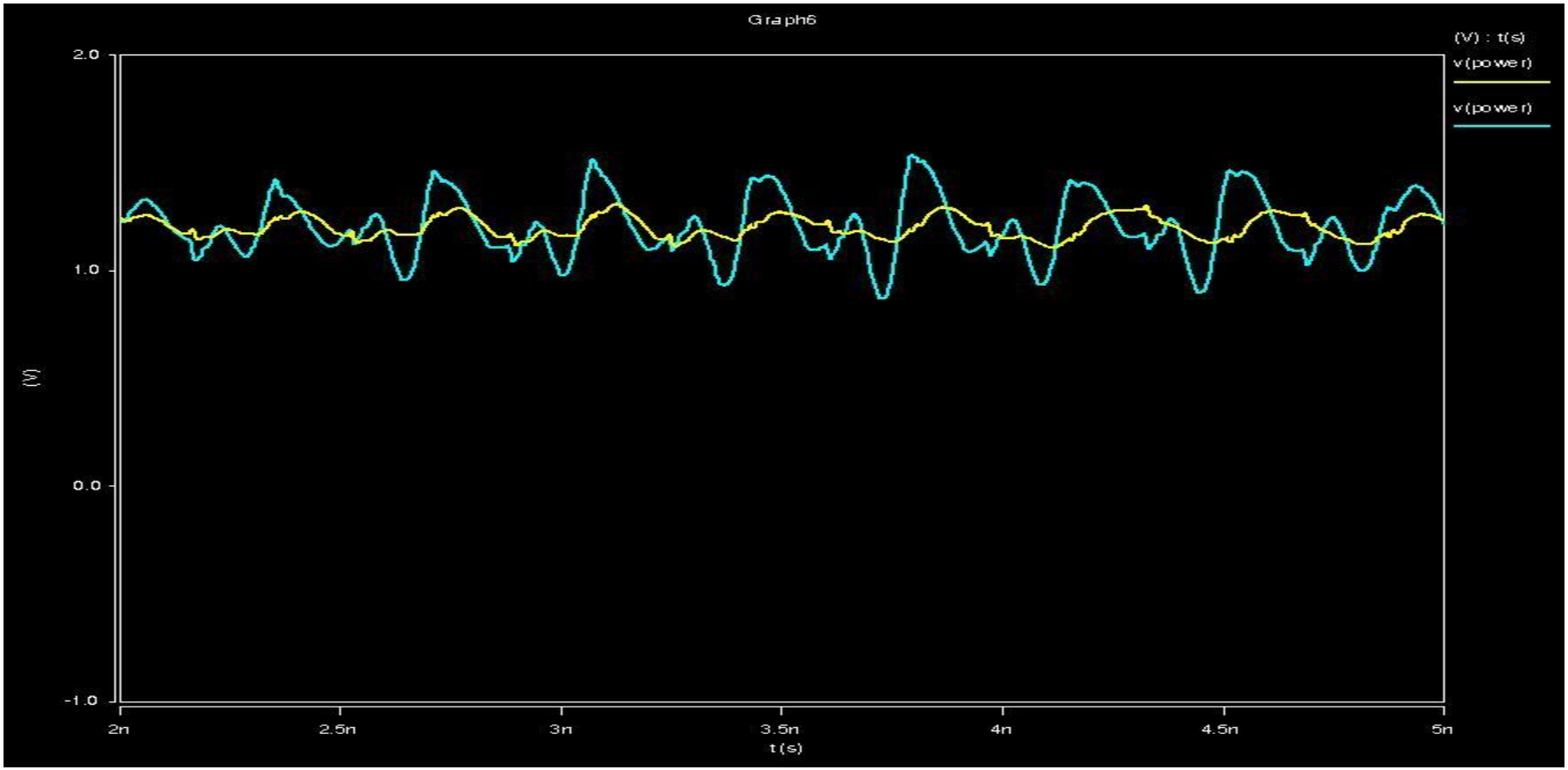


Inverter Revised Results



Yellow- Inverter HSPICE Simulation Blue- Inverter Revised Simulation

16-Stage Fibonacci Revised Results

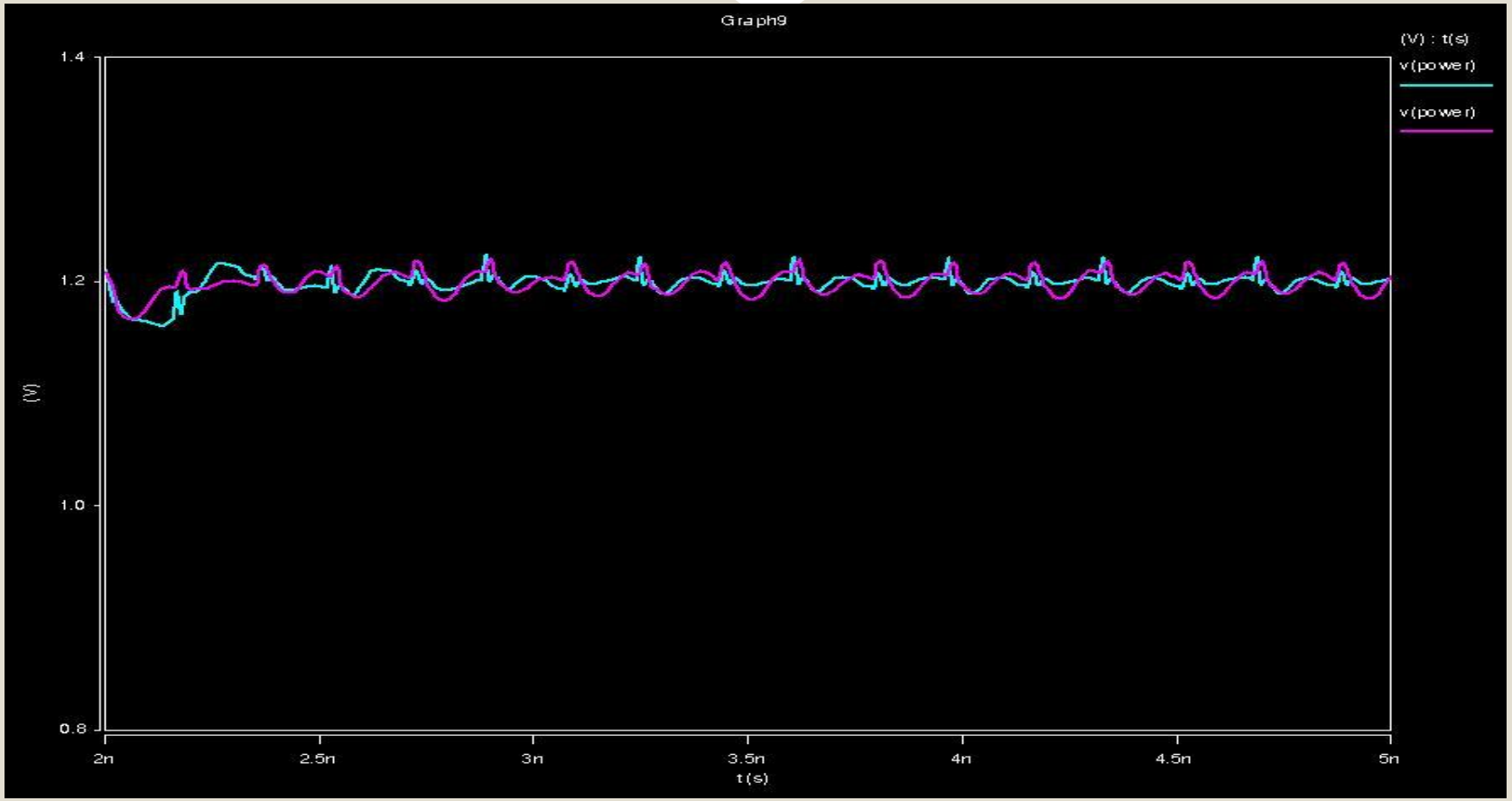


Yellow- HSPICE Simulation Blue- 16 Stage Fibonacci Revised

Revised Configuration Results

- Cleaner Power and Ground voltage waveforms
- Pretty accurate compared to HSPICE results
- Still required circuit modifications

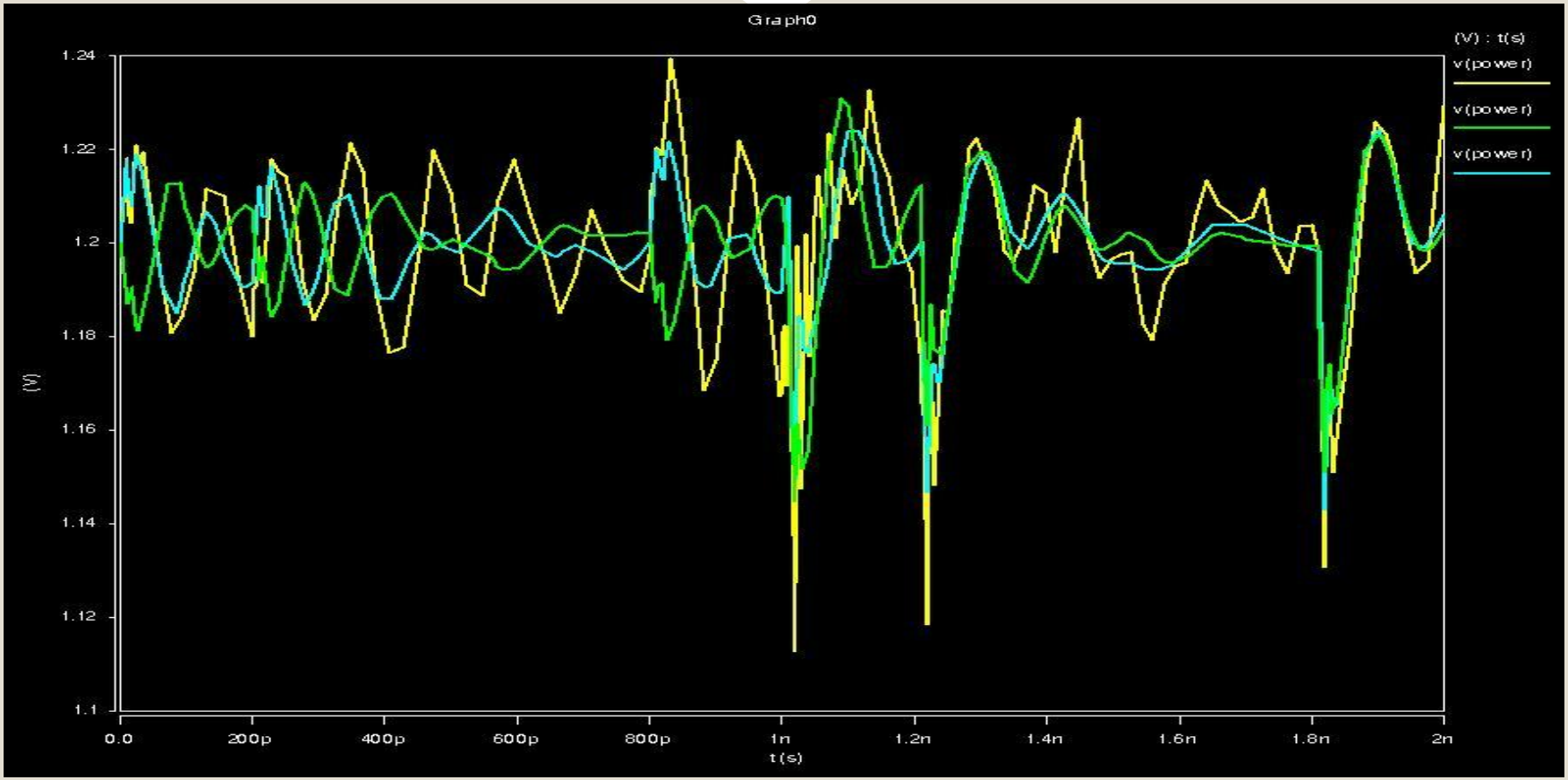
Comparison With Multi-Phase Results



Blue- End of 1st Iteration 4-Stage Fibonacci

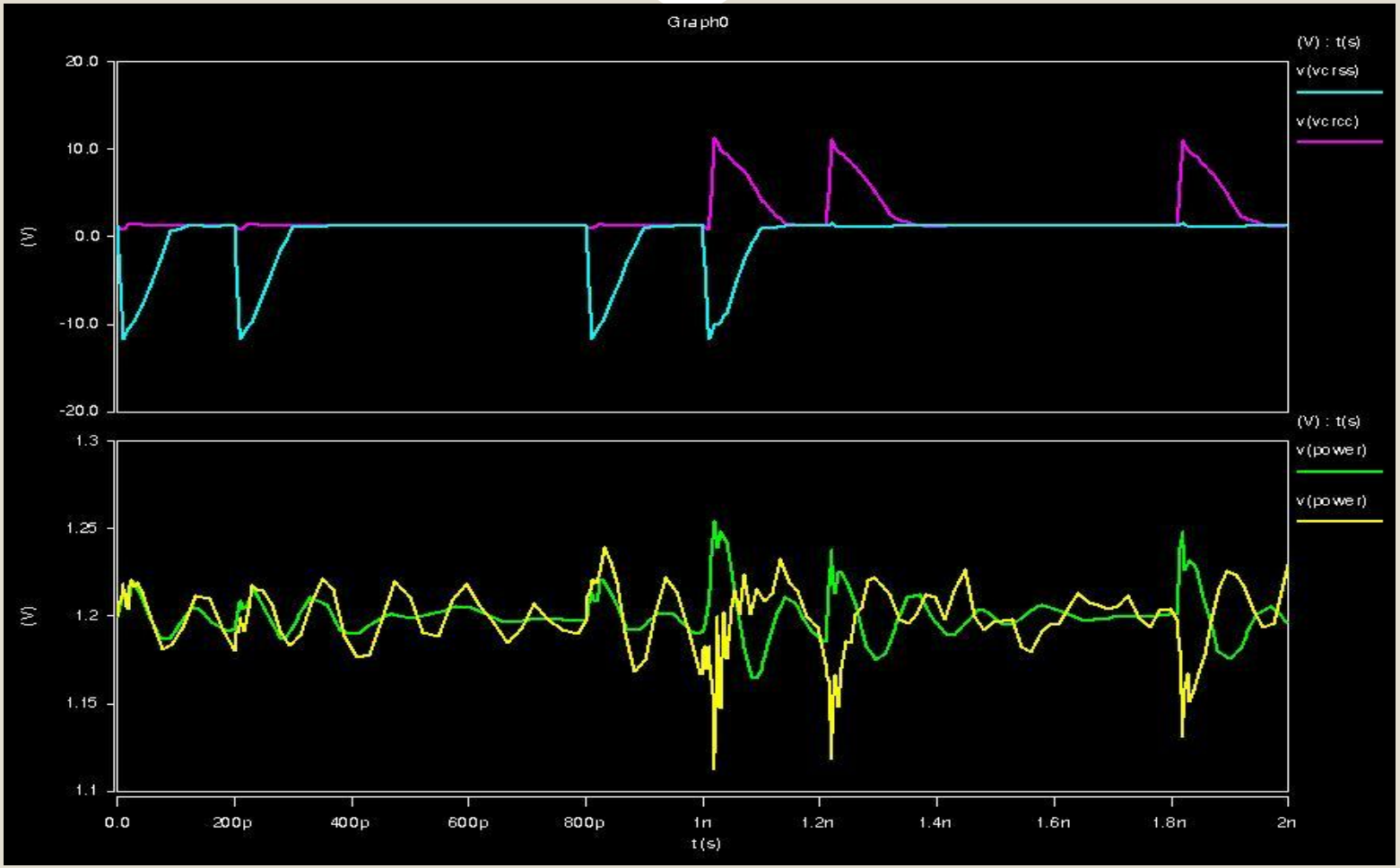
Purple-Revised 4-Stage Fibonacci Results

Inverter Comparison



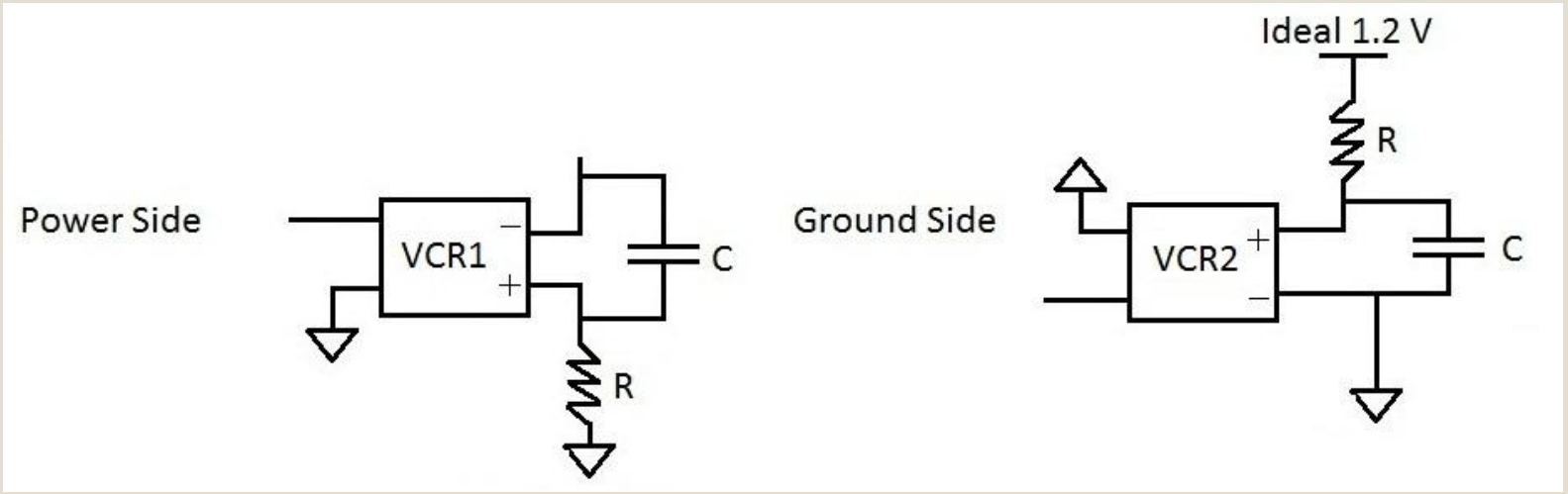
Blue– Revised Green- End of 1st Iteration Results Yellow- HSPICE Results

Practical Configuration

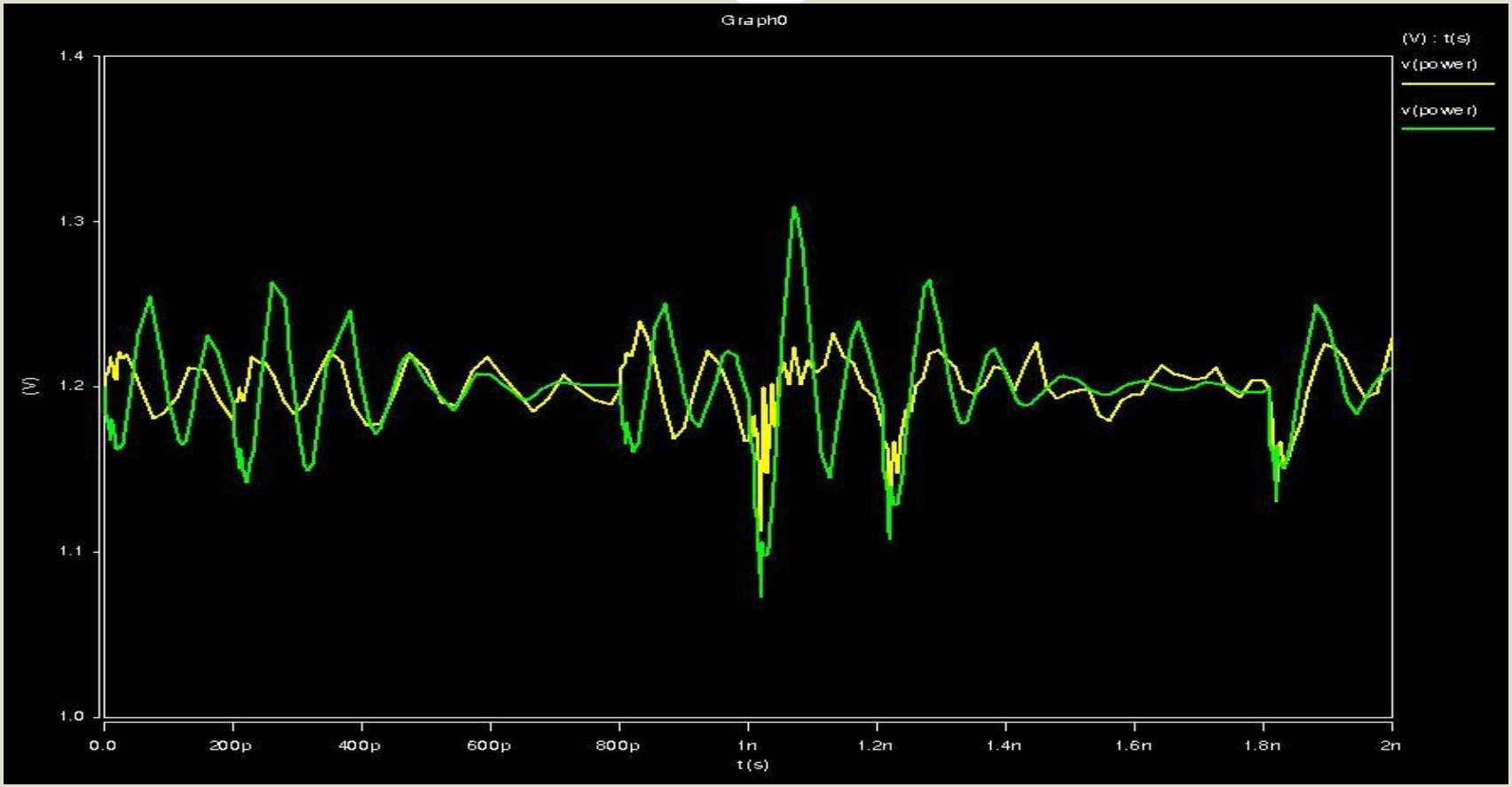


Practical Configuration

- Determined that VCRCC voltage was effecting the voltage swings
  - Switched Polarity of VCR1

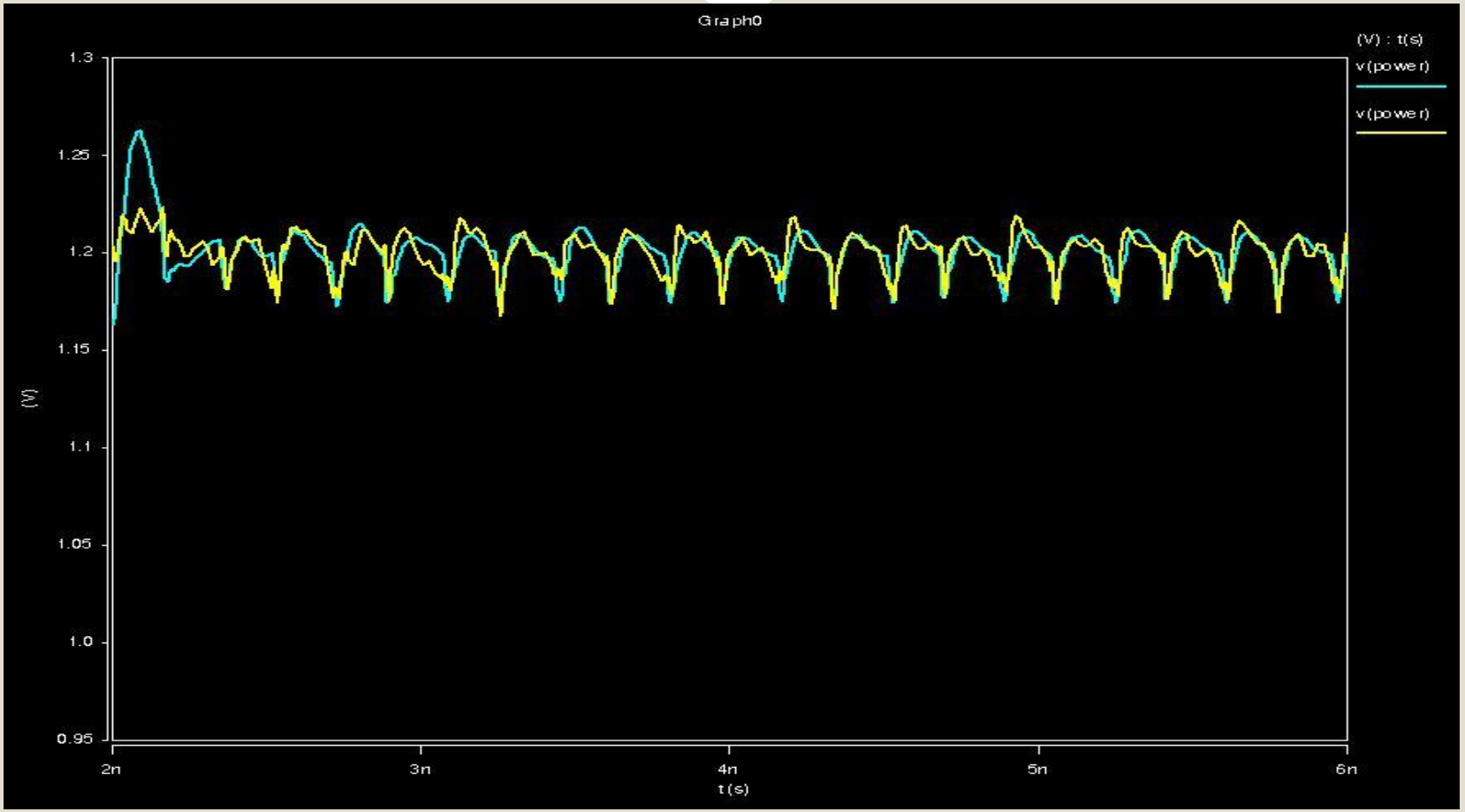


Inverter Practical Results



Green- Universal Results Yellow- HSPICE Results

4-Stage Fibonacci Practical Results



Yellow- 4-Stage Fibonacci Universal Results Green- HSPICE Results

Practical Configuration Results

- No modifications were needed from circuit to circuit
- Still some inconsistency remained with Inverter results
  - Phase shifts at the from 0 to 400 ps
  - Can not match voltage swings throughout the simulation
- Not as accurate and slower than HSPICE baseline
- Simulation runtimes were same to the initial configuration

Simulation Runtimes

Initial Configuration

	Real	User	Sys
Inverter	15.52	15.1	0.07
Adder	78.61	78.13	0.11
Fib 4	95.67	44.92	0.1
Fib 8	115.41	114.73	0.1
Fib 16	161.75	161.19	0.14
Multi	53.88	53.39	0.09

Revised Configuration

	Real	User	Sys
Inverter	21.69	20.58	0.1
Adder	110.2	109.14	0.7
Fib 4	135.9	135.9	0.44
Fib 8	692.75	690.62	0.73
Fib 16	549.17	548.17	0.63
Multi	149.53	148.17	0.83

Comparison with Multi-Phase Results

Revised Configuration

	Real	User	Sys
Inverter	21.69	20.58	0.1
Adder	110.2	109.14	0.7
Fib 4	135.9	135.9	0.44
Fib 8	298.33	300.29	0.73
Fib 16	549.17	548.17	0.63
Multi	149.53	148.17	0.83

End of 1st Iteration of Multi-Phase

	Real	User	Sys
Inverter	38.06	36.68	0.1
Adder	153.2	145.57	0.44
Fib 4	472.62	469.28	1.8
Fib 8	344.65	342.28	1.48
Fib 16	654.89	612.88	4.6
Multi	254.66	236.15	0.83

Comparison with HSPICE Runtimes

Revised Configuration

	Real	User	Sys
Inverter	21.69	20.58	0.1
Adder	110.2	109.14	0.7
Fib 4	135.9	135.9	0.44
Fib 8	298.33	300.29	0.73
Fib 16	549.17	548.17	0.63
Multi	149.53	148.17	0.83

HSPICE Simulation Package + Die

	Real	User	Sys
Inverter	20.77	19.29	0.08
Adder	78.05	76.7	1.13
Fib 4	117.83	117.05	1.1
Fib 8	200.4	199.5	0.45
Fib 16	321.16	314.21	1.2
Multi	132.14	131.08	0.87

Future Considerations

- Integrating the VCR model into the Multi-Phase simulation method
- Work on replacing each transistor within each circuit with a VCR and analyze the effects
- Run our work through HSIM^{plus} and compare with results taken with HSPICE

Group Conclusions

- Successful Scripting for accurate data points
- Multi-Phase Conclusions:
  - Complicated capacitance values = much slower run-times
  - Multiple iterations resolved to the wrong values
- VCR Creation Conclusions:
  - Able to reproduce simple currents
  - Able to replace current source
- Two-Phase VCR Method
  - Accurate but not as fast as HSPICE
  - Required circuit modifications
  - Despite universal configuration, still failed

Any Questions?

References:

[1] 2009-2010 Micron Clinic Team, “Evaluation of Integrated Circuit Power Supply Noise with Two-Phase Analysis.”, April 2009

[2] Tim Hollis, "University of Utah Senior Clinic 2009-2010". [PowerPoint Presentation]. April 10, 2009

[3] “Voltage Controlled Resistor”, January 2011 <http://www.ecircuitcenter.com/circuits/vc_resistor1/vc_resistor1.htm>

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