Leakage and Capacitance Optimized SCR Based ESD Protection Structures for Precision Analog IC Applications

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1. Abstract

Traditional ESD protection structures experience leakage current and/or capacitive loading that is undesirable for many precision analog IC applications such as charge amplifiers, transimpedance amplifiers, and x-ray detectors. Therefore, these sensitive applications suffer conflicting trade-offs between ESD protection and performance. This work proposes several novel SCR based ESD protection structures intended to provide optimized leakage and capacitive loads while maintaining competitive levels of ESD immunity. A parasitic loading model was developed to predict and simulate the performance of each proposed structure.

2. Introduction

2.1 Background

Most people don't think that static electricity is more than the little shock experienced when they touch a metal doorknob after walking across a carpeted room. However, static electricity has been an issue of great concern for hundreds of years. Protection against electrostatic discharge (ESD) started as early as in the fifteenth century with European military agencies using static control procedures and devices to prevent ESD ignition of black powder and munitions.[1]

The age of electronics brought with it a new complexity with respect to ESD protection, and as devices became smaller their sensitivity to ESD increased.[2] Therefore, the electronics industry has been and continues to be greatly concerned with ESD immunity. Even with a great deal of effort in the past decade, ESD persists to have a great impact on production yields, manufacturing costs, product quality, product reliability, and profitability. It has been estimated that ESD damage costs the industry an average of fifteen billion dollars a year.[3]

ESD failure is a very profound reliability problem for integrated circuits (IC) and poses a great challenge to the semiconductor industry.[4] As Figure 1 shows, IC parts are extremely susceptible to ESD damage and along with electrical over-stress (EOS), of which ESD is a subset, contribute up to 37% of all IC failures.[5]

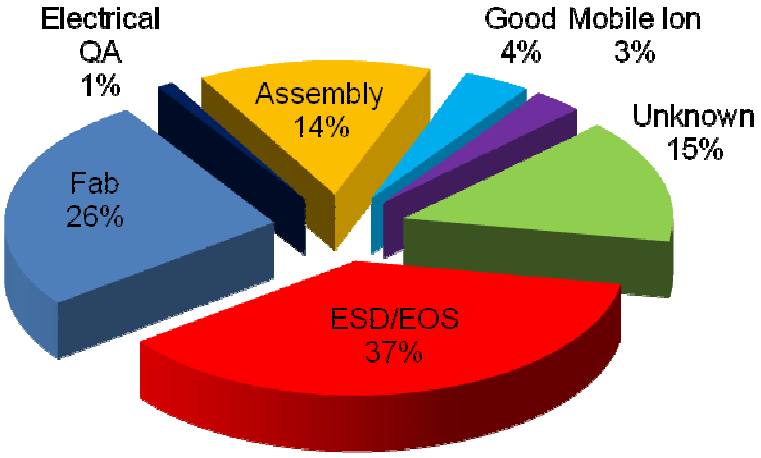

Figure 1: Distribution of failure models in silicon ICs

The two main ESD failure mechanisms in ICs are associated with thermal damages and dielectric failures. Thermal damage is directly related to the heat generated with the extremely large currents of the ESD event. Due to the poor thermal conductivity of silicon and the transient nature of the ESD events, the heat has little chance to be dissipated and results in highly localized thermal defects. On the other hand, dielectric failures are caused by the high electric field induced dielectric breakdown resulting from the great voltages produced by the ESD event.[6]

When an IC is exposed to an ESD event it may experience a catastrophic failure, where the device is permanently damaged. But more commonly, the ESD event may cause the device to experience latent defects, leaving the device partially degraded yet capable to perform its intended function. The operating life of the device is often times dramatically reduced and premature failure may occur after the user places the device in

service. Such failures can be extremely costly to repair and may create personnel hazards.[7]

2.2 ESD Protection

There are two main mechanisms to protect against ESD events: dissipate the ESD transient current and clamp the ESD voltage pulse.[8] The first of these two is necessary in order to avoid the effects of thermal damage and is done by providing a low-impedance discharge path for the large currents. The later is important to avoid dielectric failures by clamping the great voltages to a safe value as quickly as possible.

Traditionally diodes have been used to provide the ESD protection required. The use of diodes as ESD protection has the advantages of being very simple to design and easy to simulate in the modern CAD tools, but also has a few disadvantages. The diode system suffers from the need to have multiple ESD buses for each rail along with the need for power clamps on the power rails. They are also very large in size in order to handle the large currents that the ESD event produces, making them have significant parasitic capacitance. This traditional method also experiences substantial leakage current when the voltage, temperature, or process parameters change from the desired value.

2.3 Problem of Interest

There are many precision analog IC applications, such as charge amplifiers, transimpedance amplifiers, and x-ray detectors, which are very sensitive to leakage current and/or capacitive loading. Therefore, the traditional ESD protection structures introduce conflicting design trade-offs between ESD immunity and circuit performance. There exists a need for improved low-leakage, low-capacitance ESD protection structures for such applications. This work proposes a series of novel silicon controlled rectifier (SCR) based ESD protection structures intended to provide optimized leakage and capacitive loading

while maintaining competitive levels of ESD immunity. A parasitic loading model was developed to predict and simulate the performance of each proposed structure.

3. Body

3.1 SCR Based Structures

SCR structures are a very attractive option for use in ESD protection structures due to their high current handling capabilities and small size. These structures have a measured ESD protection capability of 80 V/µm[9] compared to the ESD protection capability of 16 V/µm[10] for the traditional structures. Therefore, SCR structures are five times more efficient than the standard approach, making them capable of having competitive ESD immunity without a lot of area. This in turn makes their capacitive loading much less than diodes. SCR structures also provide the advantage that they don't require more than one structure per input/output (IO) pad, only necessitate one ESD bus, and don't call for any power clamps. All of these allow the total area used for ESD protection on the IC to be significantly reduced. SCR structures can also be designed to have extremely low leakage current, making this type of structure the obvious choice for the design goals of this body of work.

Although SCR structures provide a lot of very attractive benefits, there are two main disadvantages associated with these structures. Due to the snap-back characteristic of the current-voltage (I-V) curve, shown in Figure 2, these structures are not easily simulated in our modern CAD tools. Customized models must be developed in order to simulate both the parasitic loading of the structure and the active snap-back action of the device. The work of developing an active snap-back model for the proposed structures has been left for future work. SCR structures also require a great deal of design time to ensure that they provide the required ESD immunity without affecting the performance of the IC. One of the most important design criteria associated with SCR based ESD protection structures is the

triggering voltage depicted in Figure 2. Careful attention is required to ensure that this voltage level is low enough to avoid ESD damage but not low enough to trigger under normal operation of the IC. This triggering voltage was optimized in each of the 5 proposed models.

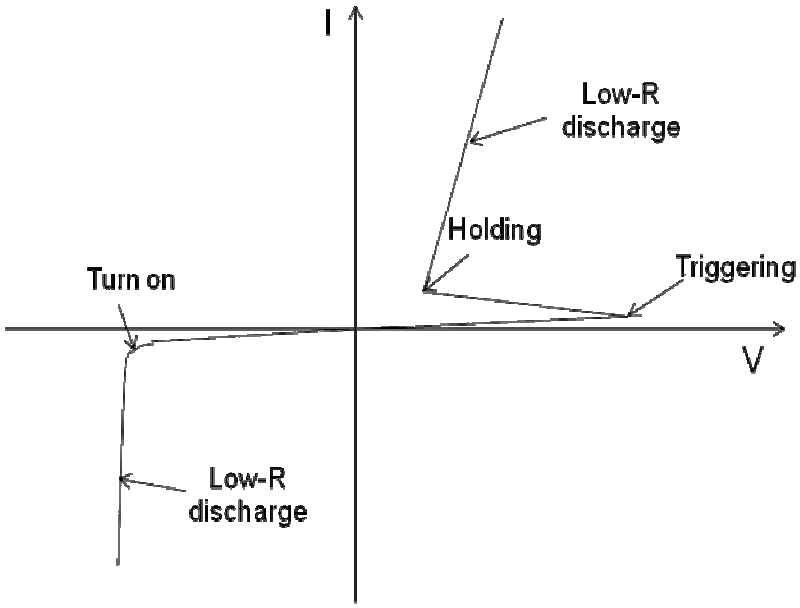

Figure 2: I-V curve of an SCR based ESD protection structure

3.2 Silicon Measured Data

A standard low-voltage SCR based ESD protection structure was fabricated in the 0.5 µm process and the silicon result was measured for DC leakage current, triggering voltage, and ESD immunity. Figure 3 is a screenshot of the layout of the ESD structure that was measured and Figure 4 is the equivalent circuit of this structure. Note that Q2 is only one device, an NMOS transistor. The lateral NPN is embedded in the NMOS and is shown here only to demonstrate the SCR structure of this device.

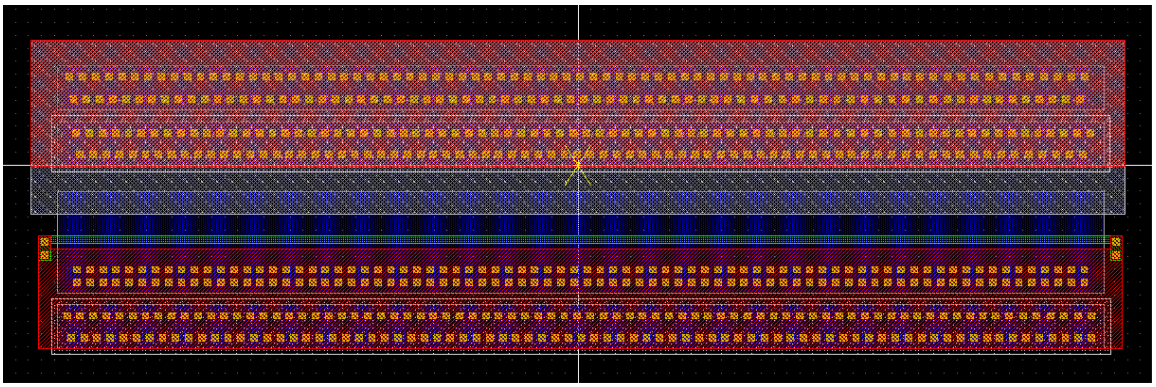

Figure 3: Layout of the silicon measured ESD structure

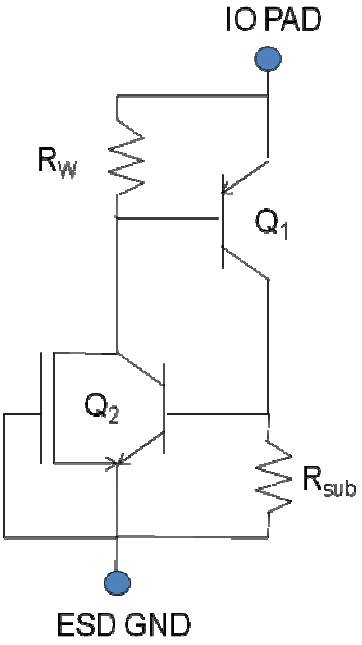

Figure 4: Equivalent circuit of the silicon measured ESD structure

The resistor R_W is the well resistance of the n-well, the PNP transistor Q1 is vertically formed, resistor R_{sub} is the substrate resistance, and Q2 is the NMOS with the embedded NPN. The NMOS wad a width of 80 µm and a channel length of 1 µm.

The measured DC leakage current of this structure was obtained at four different temperatures and can be found in Table I. Only four values were obtained due to the great

difficulty in accurately measuring such low current values across such a large temperature range.

Table I: Silicon measured DC leakage current

Temperature	Leakage Current
25 ℃	364 fA
40 ℃	1.68 pA
70 ℃	21.2 pA
125 ℃	1.91 nA

The triggering voltage of this structure was found by performing a transmission-line-pulsing (TLP) test. The results of that test show the snap-back action of the structure and clearly show that the triggering voltage was at 14 V, as can be seen in Figure 5.

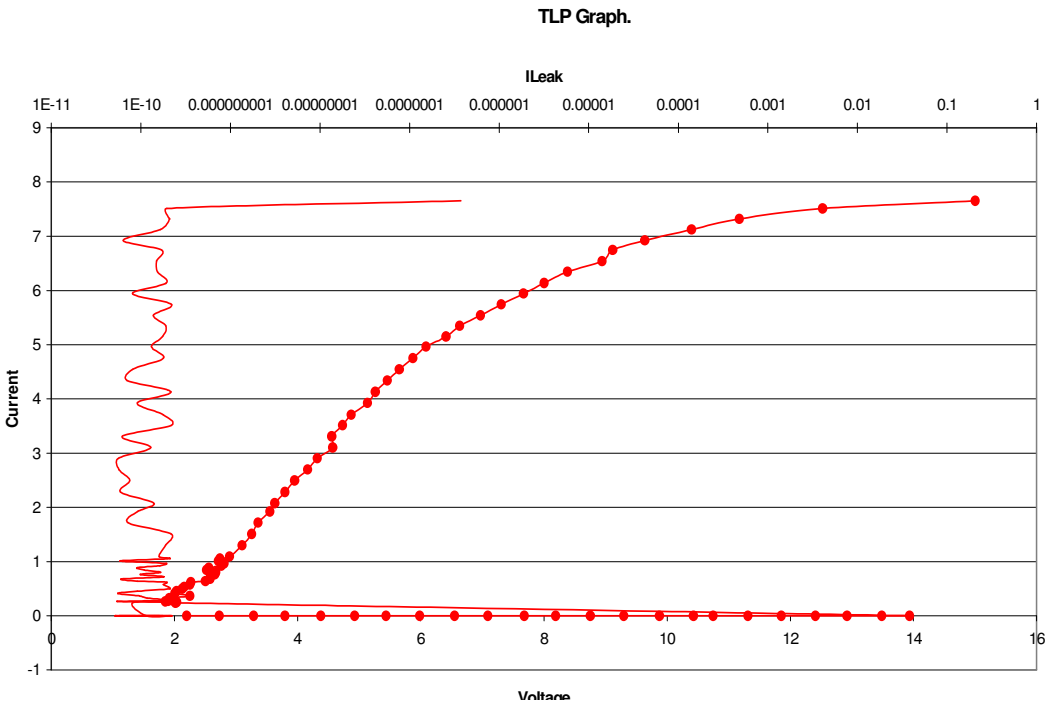

Figure 5: Measured TLP graph showing the 14 V triggering voltage

This SCR based ESD protection structure was measured for ESD immunity and showed that it could handle a 4 kV human body model (HBM) ESD pulse without causing any damage to the IC.

3.3 Simulations

3.3.1 Leakage Current

For each of the proposed models and the control model, the leakage current was simulated using Virtuoso Spectre Circuit Simulator. This was done by taking the device under test (DUT) and applying a 2 V DC voltage source across the structure, maintaining the same configuration used when collecting the measured silicon data. A DC simulation was then performed with the temperature varied from 0 ℃ to 140 ℃ and the current through the DUT was measured and saved. This yielded the predicted leakage current of the DUT.

3.3.2 Capacitive Loading

For each of the proposed models and the control model, the capacitive loading was simulated using Virtuoso Spectre Circuit Simulator. This was done by first assuring that the initial conditions of the DUT were all set to zero and then applying a current pulse across the structure. The magnitude and period of the pulse were determined by verifying that the voltage across the structure had enough time to settle to a steady-state value. A transient simulation was then performed and the voltage across the DUT was measured and saved. The slope of the voltage was found from the point of the initial current pulse up until the voltage was nearly settled. The capacitance was then found by taking the value of the current pulse divided by the slope of the voltage. This was done at room temperature, resulting in the predicted capacitive loading of the DUT.

3.3.3 Startup Current

This work uses the startup current as a prediction of how quickly the structure will trigger, which qualitatively depicts the amount of ESD immunity the device will have. For each of the proposed models and the control model, the startup current was simulated using Virtuoso Spectre Circuit Simulator. This was found by applying a simulated HBM

ESD pulse of 1 kV across the DUT. A transient simulation was then performed and the max current through the DUT was measured and saved. This was done at room temperature, resulting in the predicted startup current of the DUT.

3.4 Control Model

The purpose of the Control Model was to provide a simulation model that closely matched the DC leakage current results of the silicon measured SCR based ESD structure. Therefore, the model was made to physically match the measured structure as seen in Figure 3 with the NMOS (Q2) having a width of 80 µm and a channel length of 1 µm. Once the device was modeled, the standard PNP model (Q1) was optimized in order for the simulated leakage results to match the measured leakage results. This process led to three customized corner models for the PNP: fast, typical, and slow. Figure 6 depicts the DC leakage current simulations for the three corners of the Control Model compared to the Measured Data.

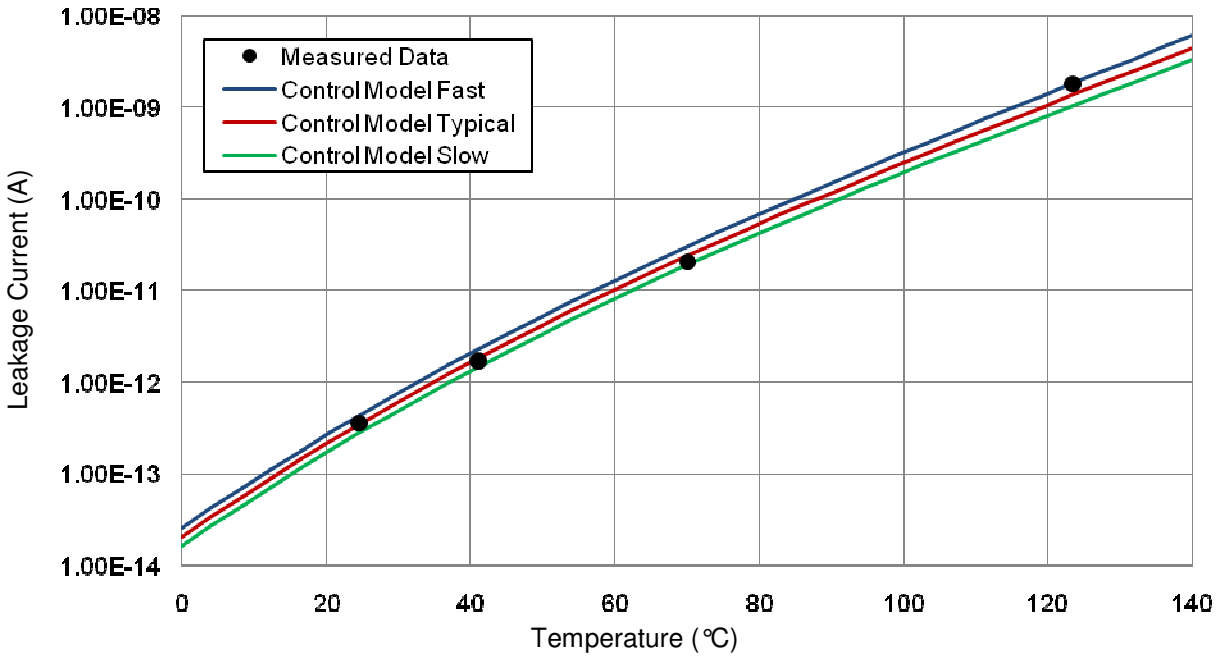

Figure 6: Simulated DC leakage current of the Control Model compared to the Measured Data

The average leakage current of this structure across temperature and with the typical corner model was found to be 503 pA. The capacitive load was then simulated and found to be 444.4 fF. The startup current of the Control Model was also simulated and the maximum was found to be 0.437 A. These three results were used as a comparative base to the other 5 proposed structures to help predict their performance. Each proposed model used the physical design of the Control Model as the base with minor adjustments made, in an effort to help improve its performance.

3.5 Proposed Model 1

This model was designed with two changes when compared to the Control Model. The first of these changes was made to the NMOS. The length was increased to 2 µm for ¾ of the width of the device and left at 1 µm for the other ¼ of the device width. The reason for the increase in length of the channel was to help reduce the amount of leakage current, but in doing this the device would not trigger as quick. Therefore, in an effort to get better leakage results without giving up ESD immunity, the channel length was modulated from 2 µm down to 1 µm and then back to 2 µm, with the 1 µm length serving as the center triggering region.

The other change was to add a resistor between the gate of the NMOS and ground in an effort to help increase the startup current and decrease the triggering voltage even more. This resistive gate tie uses the built in gate-to-drain capacitance (C_{gd}) of the NMOS to RC couple the gate to the I/O pad of the structure. Therefore, when the IO pad experiences a positive ESD event, the RC coupling turns on the NMOS relatively quick and the triggering voltage of the device is significantly reduced which greatly increases the startup current. Figure 7 contains a screenshot of the layout of this structure.

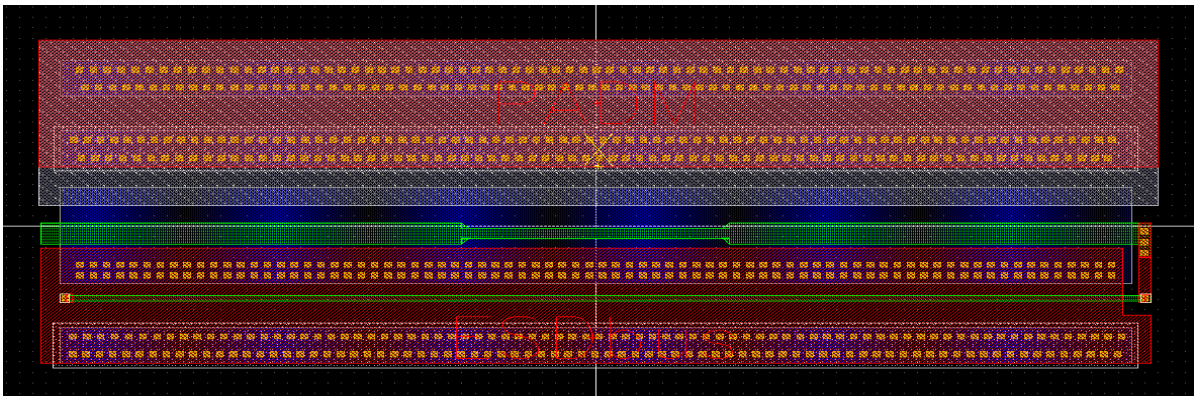

Figure 7: Layout of the Proposed Model 1

The leakage current simulation of this structure produced encouraging results. The average leakage current across temperature and with the typical corner model of the PNP was found to be 363 pA, which yielded a 27.8% improvement over the Control Model. The capacitive load was simulated to be 251.3 fF, which was found to be 43.5% less than the capacitive load of the Control Model. Finally, the startup current was simulated and the maximum was found to be 0.517 A, an 18.3% increase over the Control Model. Overall, this proposed model had significant improved performance in leakage current, capacitive loading, and startup current. Moreover, a predictive parasitic model was developed for this structure.

3.6 Proposed Model 2

This model was designed with two changes when compared to the Control Model. The first of these changes was made to the NMOS. The channel length was maintained at 1µm but the width of the transistor was decreased from 80 µm to 20 µm, in an effort to decrease the amount of leakage current. This change in width would significantly lower the beta product of the lateral NPN which in turn would increase the trigger voltage. Therefore, in an effort to substantially decrease the leakage current without giving up competitive ESD immunity, this minimal trigger NMOS was maintained and a resistive gate tie was added to this structure. This resistor between the gate of the NMOS and ground was designed to

have the same effect as explained in section 3.5. Figure 8 contains a screenshot of the layout of this structure.

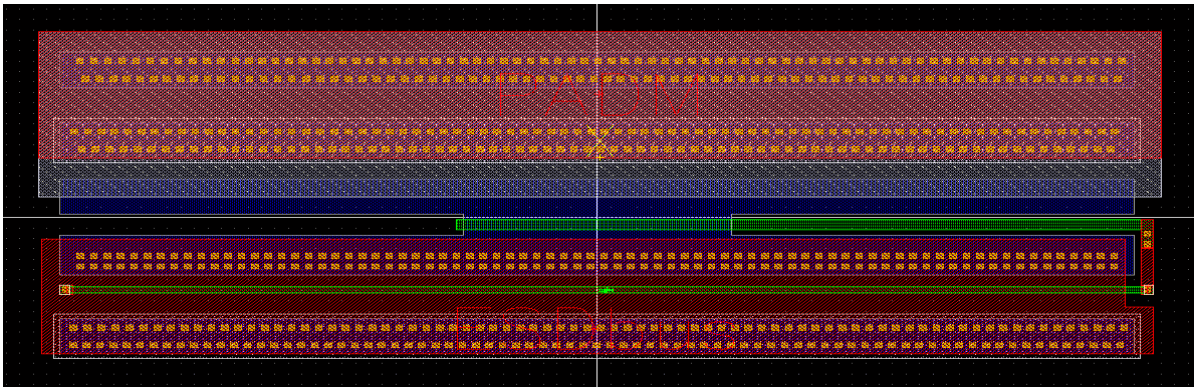

Figure 8: Layout of the Proposed Model 2

The leakage current simulation of this structure produced very encouraging results. The average leakage current across temperature and with the typical corner model of the PNP was found to be 208 pA, which yielded a 58.6% improvement over the Control Model. The capacitive load was simulated to be 243.0 fF, which was found to be 45.3% less than the capacitive load of the Control Model. Finally, the startup current was simulated and the maximum was found to be 0.446 A, a meager 2.06% increase over the Control Model. Overall, this proposed model had significant improved performance in leakage current and capacitive loading with very little improvement in startup current. Moreover, a predictive parasitic model was developed for this structure.

3.7 Proposed Model 3

This model was designed with only one minor change when compared to the Control Model. The only change was the addition of a resistive gate tie to the NMOS with the desire to improve the startup current but not change the leakage current performance. Therefore, this model was expected to perform very similarly to the Control Model but with better ESD immunity. Figure 9 contains a screenshot of the layout of this structure.

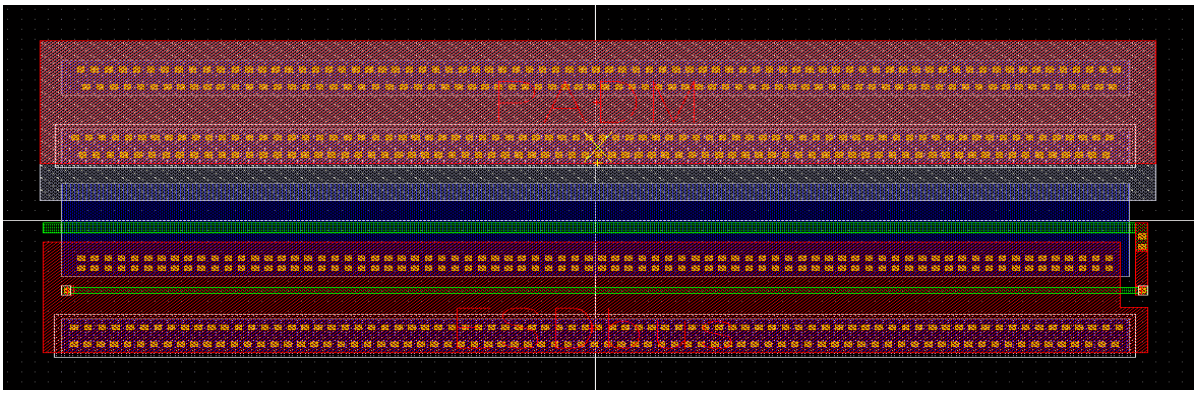

Figure 9: Layout of the Proposed Model 3

As expected, the leakage current simulation of this structure produced the same results as the Control Model. Therefore, the average leakage current across temperature and with the typical corner model of the PNP was found to be 503 pA, which yielded a 0% improvement over the Control Model. The capacitive load was simulated to be 292.4 fF, which was found to be 34.2% less than the capacitive load of the Control Model. Finally, the startup current was simulated and the maximum was found to be 0.524 A, an increase of 19.9% over the Control Model. Overall, this proposed model had significant improved performance in startup current and capacitive loading with no improvement in leakage current. Moreover, a predictive parasitic model was developed for this structure.

3.8 Proposed Model 4a

This structure was designed with two changes when compared to the Control Model. The first of these changes was made to the NMOS. The channel length of this device was increased from 1µm to 2 µm across its entire width. This was done in an effort to decrease the leakage current, but also aided to decrease the startup current. Therefore, in order to increase the startup current, a capacitor was added between the IO pad and the gate of the NMOS along with the addition of a resistive gate tie. This was intended to have much more effect than the RC coupling technique described in section 3.5 because the discrete

capacitor could be made large enough to turn the transistor on longer. Figure 10 contains a screenshot of the layout of this structure.

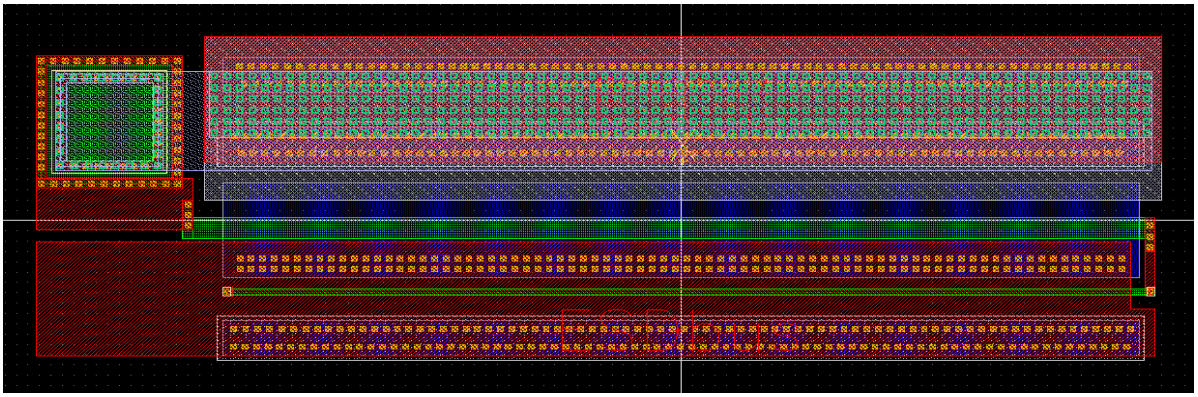

Figure 10: Layout of the Proposed Model 4a

The leakage current simulation of this structure produced very encouraging results. The average leakage current across temperature and with the typical corner model of the PNP was found to be 318 pA, which yielded a 36.8% improvement over the Control Model. The capacitive load was simulated to be 1.25 pF, which was found to be 181.3% more than the capacitive load of the Control Model due to the added capacitor. Finally, the startup current was simulated and the maximum was found to be 0.601 A, a 37.5% increase over the Control Model. Overall, this proposed model had significant improved performance in leakage current and startup current but significantly worse capacitive loading. Moreover, a predictive parasitic model was developed for this structure.

3.9 Proposed Model 4b

This structure was designed with two changes when compared to the Control Model and only a small change when compared to the Proposed Model 4a. The change was made in the length of the NMOS device. The channel length was increased from 2 µm to 4 µm in an effort to decrease the leakage current even more than the previous structure. The capacitor from the IO pad to the gate of the NMOS and the resistive gate tie were

maintained as in the previous structure. Figure 11 contains a screenshot of the layout of this structure.

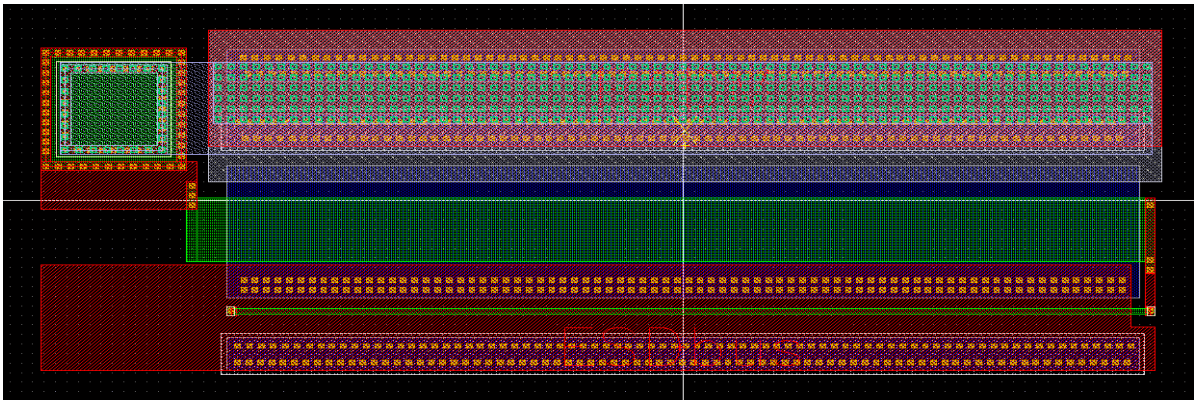

Figure 11: Layout of the Proposed Model 4b

The leakage current simulation of this structure produced very encouraging results. The average leakage current across temperature and with the typical corner model of the PNP was found to be 250 pA, which yielded a 50.3% improvement over the Control Model. The capacitive load was simulated to be 1.33 pF, which was found to be 199.3% more than the capacitive load of the Control Model due to the added capacitor. Finally, the startup current was simulated and the maximum was found to be 0.598 A, a 36.8% increase over the Control Model. Overall, this proposed model had significant improved performance in leakage current and startup current but significantly worse capacitive loading. Moreover, a predictive parasitic model was developed for this structure.

3.10 Proposed Model 5

This structure was designed with only one modification when compared to the Proposed Model 3. The change was made by turning the source of the NMOS from an N+ diffusion in the P-substrate to an N+ diffusion sitting in an N-well. This was done in an effort to increase the beta product of the lateral NPN with the hope of decreasing the trigger voltage. This structure was not simulated because the simulation tools available are not capable of

simulating the intended affect. Figure 12 contains a screenshot of the layout of this structure.

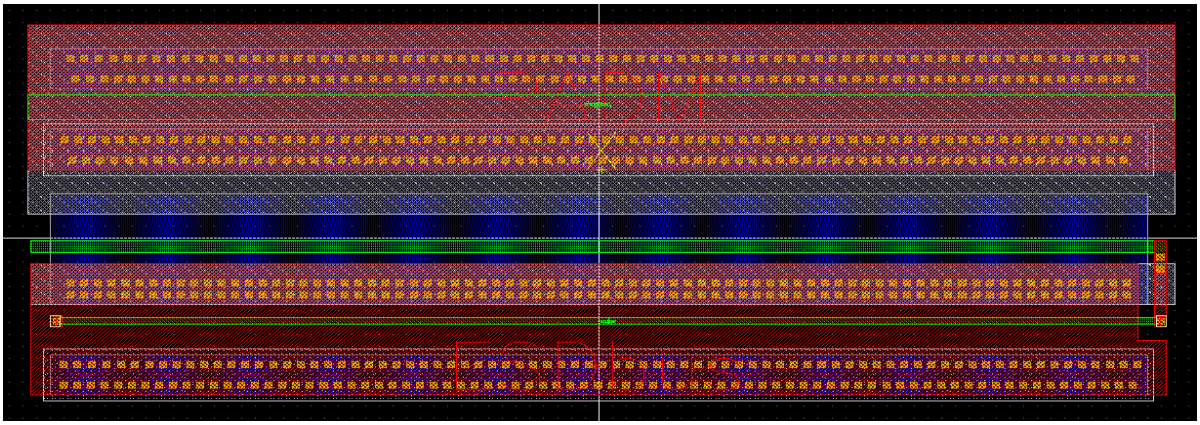

Figure 12: Layout of the Proposed Model 5

4. Conclusion

This work has presented six novel SCR based ESD protection structures intended to provide optimized leakage current and capacitive loading while maintaining competitive levels of ESD immunity. These structures can be used to provide adequate ESD protection without performance loss to precision analog IC applications. The simulated leakage current, startup current, and loading capacitance of each proposed model has been presented in an effort to predict the behavior of each structure. The simulated typical DC leakage current for each of the models compared to the Control Model can be seen in Figure 13. Note that the Proposed Model 5 was not simulated due to the inability of the tools to simulate the intended behavior.

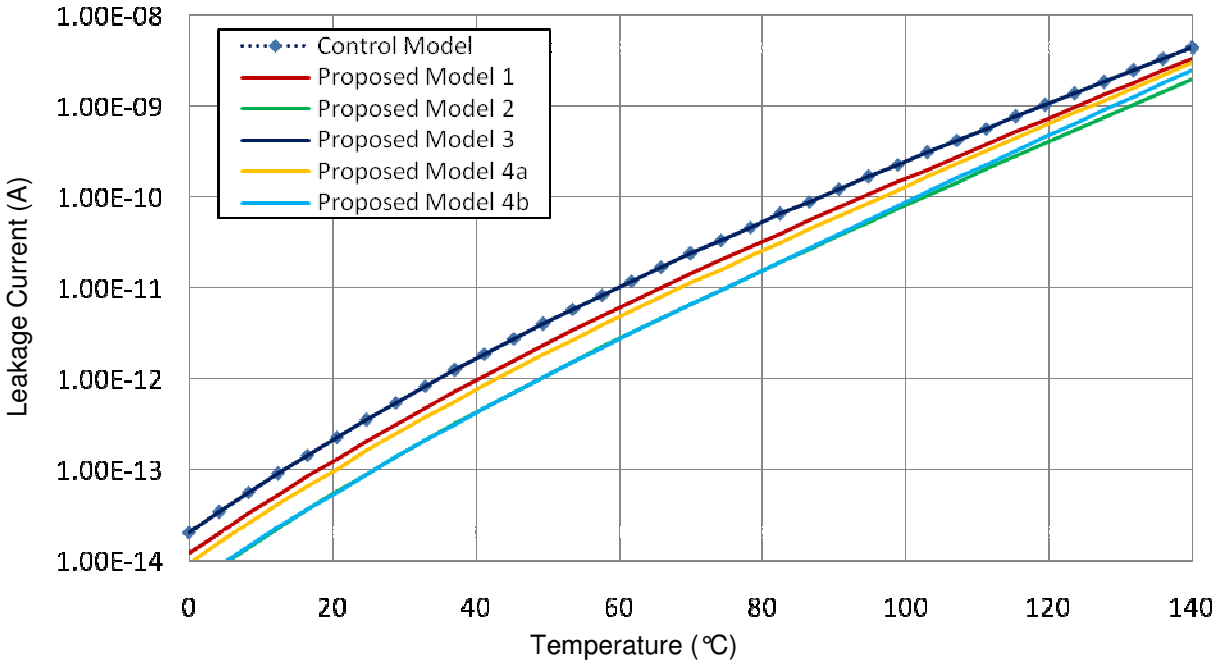

Figure 13: Simulated typical DC leakage current for each of the Proposed Models compared to the Control Model

The simulated startup current for each of the Proposed Models is shown in Figure 14 and has been used to predict how quickly the structure will trigger, which qualitatively depicts the amount of ESD immunity the device will have.

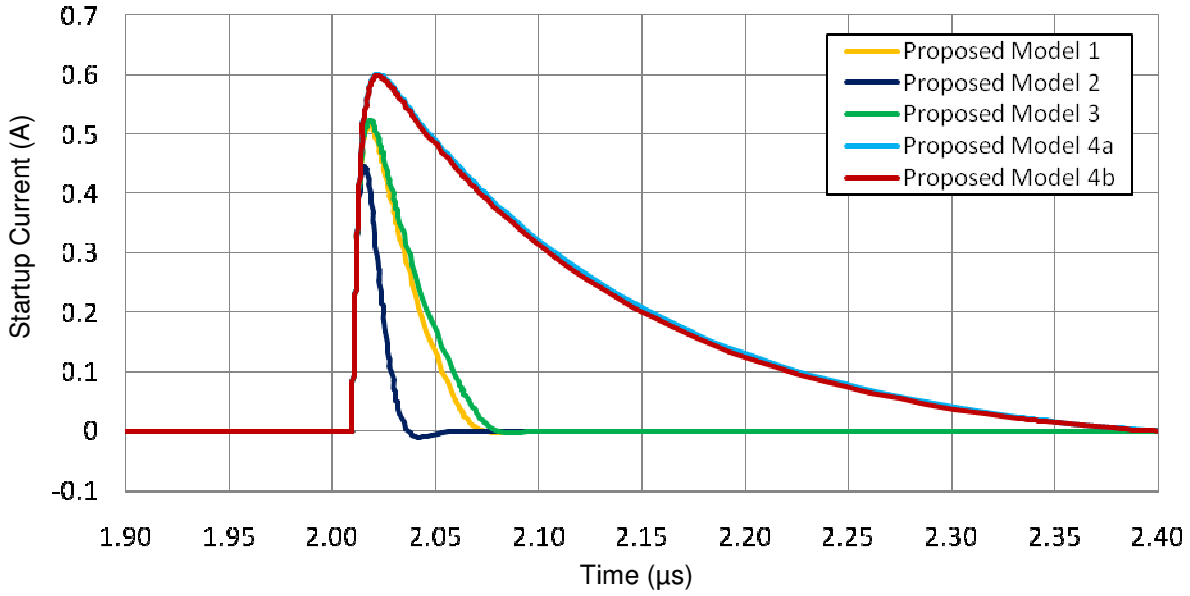

Figure 14: Simulated startup current for each of the Proposed Models

A summary of simulation results for all Proposed Models can be found in Table II. This table depicts the simulation value along with the percentage of improvement over the Control Model for each of the three simulations performed.

Table II: Summary of simulation results

Model	Avg. Leakage Current	Leakage Current Improvement	Peak Startup Current	Startup Current Improvement	Cap Loading	Cap Loading Improvement
1	363 pA	27.8 %	0.517 A	18.3 %	251.3 fF	43.5 %
2	208 pA	58.6 %	0.446 A	2.06 %	243.0 fF	45.3 %
3	503 pA	0.0 %	0.524 A	19.9 %	292.4 fF	34.2 %
4a	318 pA	36.8 %	0.601 A	37.5 %	1.25 pF	-181.3 %
4b	250 pA	50.3 %	0.598 A	36.8 %	1.33 pF	-199.3 %

Proposed Models 1 and 2 accomplished the goals of this work by providing improved leakage current and capacitive loading without sacrificing ESD immunity (startup current). Model 1 has more leakage current than Model 2 but has a substantially greater predictive ESD immunity. Therefore, if the ESD requirements are not very strict for a given application, Model 2 would provide the best leakage current and capacitive loading. Moreover, Model 1 would be the best option for leakage current and capacitive loading if the ESD requirements were more stringent. The third Proposed Model doesn't appear to be a very attractive option compared to the first two. Models 4a and 4b don't meet the goals of this project due to their increase in loading capacitance, but would be an attractive option if leakage current and ESD immunity were the most important features of the application. Therefore, the goals of this work were accomplished by proposing novel SCR based ESD protection structures with optimized leakage current and capacitive loading along with competitive ESD immunity. Parasitic loading models for each of the proposed structures were developed to predict and simulate the behavior of each model. The chip

level layout can be found in Figure 15. As can be seen, a scribe line monitor (SLM) was constructed in an effort to facilitate the ease of fabrication and test. Each of the six Proposed Models was included with the ability to test each structure completely isolated from the other structures. This layout passed Calibre DRC and LVS tests and is planned on being fabricated and tested during the summer.

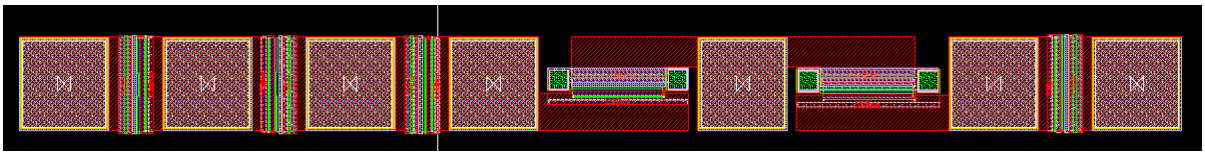

Figure 15: Layout of the entire chip

Acknowledgments

Matthew A. Tyler of ON Semiconductor (American Fork, UT 84003) assisted with this project. He provided the measured silicon results of the standard SCR based ESD structure. His insight and experience aided in developing the five proposed models. The simulation results and the parasitic loading models were approved by him.

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