CAD of Digital Circuits - Logic Synthesis & Optimization
Spring 2019 - Course Syllabus

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1) **Introduction**
   - Intro to VLSI CAD & Logic Synthesis
   - Graph Theory & Optimization problems
   - Boolean Algebra
   - Boolean Function Representation & Manipulation: BDDs
   - Satisfiability & Graph Covering
2) **Exact & Heuristic Two-Level Logic Minimization**
   - SOP & POS forms: Costs & Characteristics
   - Implicants, Cubes and Covers
   - Quine-McCluskey Method
   - Minimum Cover via Unate Covering, Branch-and-Bound Methods
   - Multi-Output Function Minimization
   - Unate Recursive Paradigm
   - The ESPRESSO Minimizer
3) **Multi-Level Logic Synthesis - Algebraic Techniques**
   - Combinational Network Representation and Transformations
   - Factored Forms and Algebraic Techniques
   - Alegbraic Division: Kernels and Co-Kernals
   - Heuristic Factoring Algorithms
   - The MIS MODEL
4) **Boolean Decomposition**
   - Functional Decomposition - Basics
   - Ashenhurst-Curtis Decomposition
   - BDS and Bi-Decomposition
   - *Don't Care* Conditions & Their Computations
   - BDD-Based Boolean Decomposition

- Decomposition for FPGAs
- New Logic Synthesis approaches based on AND-Invert Graphs and Boolean Decomposition
- The ABC Synthesis & Verification tool

5) **Delay Optimization**

- Timing Analysis - Basics
- False Path Analysis
- Circuit Restructuring for Timing Optimization
- Redundancy and Delay: KMS Algorithm

6) **Sequential Logic Optimization**

- Finite State Machine Minimization
- Two-Level Encoding: DIET & NOVA
- Multi-Level Encoding: JEDI
- Retiming of Sequential Circuits
- Retiming, Resynthesis and *Don't Cares*

7) **Technology Mapping**

- Tree & DAG Covering
- Standard Cell Mapping
- And-Invert Graphs
- Tech-mapping on FPGAs

8) **New Directions in Logic Synthesis**

- Limitations of Conventional Synthesis Tools
- Multi-Valued Logic Synthesis
- Reversible & quantum logic?
- Anything else you have in mind.....