Spartan3E Conflicts

(Note: this information, including the pictures, is taken from Spartan-3E FPGA Starter Kit Board User Guide).

LCD and Intel StartaFlash

As shown in Figure 5-1, the four LCD data signals are also shared with StrataFlash data lines SF_D<11:8>. As shown in Table 5-2, the LCD/StrataFlash interaction depends on the application usage in the design. When the StrataFlash memory is disabled (SF_CE0 = High), then the FPGA application has full read/write access to the LCD. Conversely, when LCD read operations are disabled (LCD_RW = Low), then the FPGA application has full read/write access to the StrataFlash memory

If the StrataFlash memory is in byte-wide (x8) mode (SF_BYTE = Low), the FPGA application has full simultaneous read/write access to both the LCD and the StrataFlash memory. In byte-wide mode, the StrataFlash memory does not use the SF_D<15:8> data lines.

Table 5-2: LCD/StrataFlash Control Interaction

SF_CE0	SF_BYTE	LCD_RW	OPERATION
1	X	X	StrataFlash disabled. Full read/write access to LCD.
X	X	0	LCD write access only. Full access to StrataFlash.
X	0	X	StrataFlash in byte-wide (x8) mode. Upper address lines are not used. Full access to both LCD and StrataFlash.

X's are don't cares.

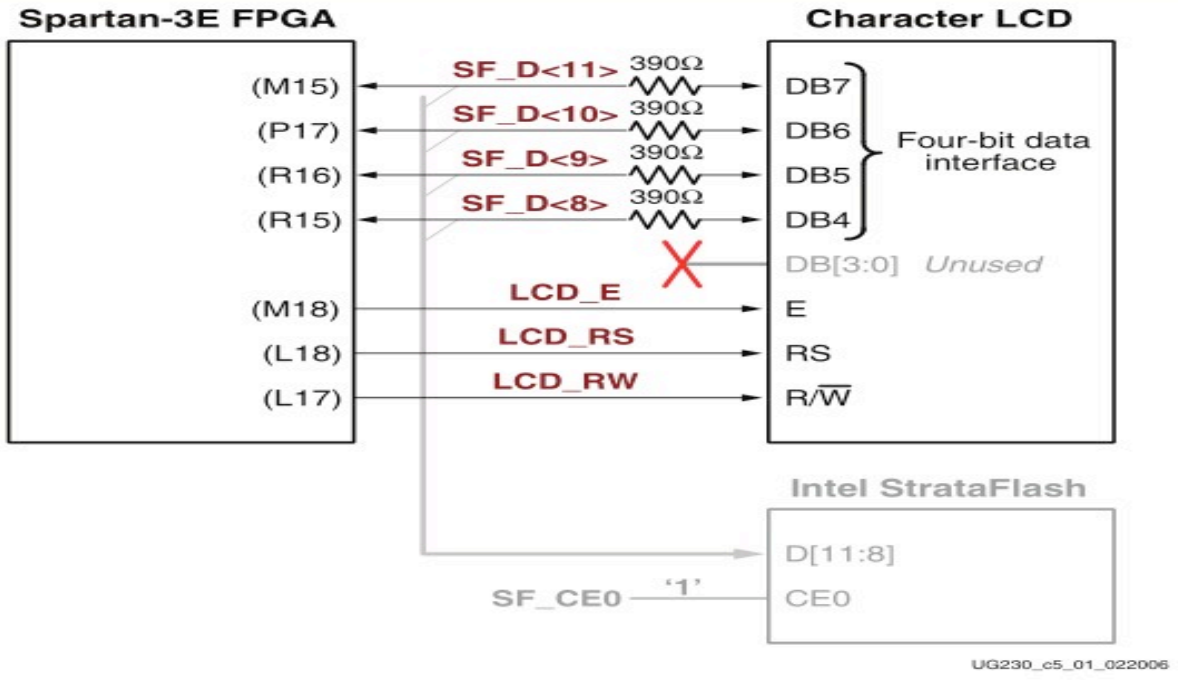

Figure 5-1: **Character LCD Interface**

Digital to Analog Converter (DAC)

Disable Other Devices on the SPI Bus to Avoid Contention:
The SPI bus signals are shared by other devices on the board. It is vital that other devices are disabled when the FPGA communicates with the DAC to avoid bus contention. Table 9-2 provides the signals and logic values required to disable the other devices. Although the StrataFlash PROM is a parallel device, its least-significant data bit is shared with the SPI_MISO signal.

Table 9-2: Disabled Devices on the SPI Bus

Signal	Disabled Device	Disable Value
SPI_SS_B	SPI serial Flash	1
AMP_CS	Programmable pre-amplifier	1
AD_CONV	Analog-to-Digital Converter (ADC)	0
SF_CE0	StrataFlash Parallel Flash PROM	1
FPGA_INIT_B	Platform Falsh PROM	1

Analog Capture Circuit (including Programmable Pre-Amplifier and Analog to Digital Converter (ADC))

Disable Other Devices on the SPI Bus to Avoid Contention:
The SPI bus signals are shared by other devices on the board. It is vital that other devices are disabled when the FPGA communicates with the AMP or ADC to avoid bus contention. Table 10-4 provides the signals and logic values required to disable the other devices. Although the StrataFlash PROM is a parallel device, its least-significant data bit is shared with the SPI_MISO signal. The Platform Flash PROM is only potentially enabled if the FPGA is set up for Master Serial mode configuration.

Table 10-4: Disable Other Devices on SPI Bus

Signal	Disabled Device	Disable Value
SPI_SS	SPI Serial Flash	1
AMP_CS	Programmable Pre-Amplifier	1
DAC_CS	DAC	1
SF_CE0	StrataFlash Parallel flash PROM	1
FPGA_INIT_B	Platform Flash PROM	1

Intel StrataFlash Parallel NOR Flash PROM

Shared Connections

Besides the connections to the FPGA, the StrataFlash memory shares some connections to other components.

Character LCD

The character LCD uses a four-bit data interface. The display data connections are also shared with the SF_D<11:8> signals on the StrataFlash PROM. As shown in Table 11-2, the FPGA controls access to the StrataFlash PROM or the character LCD using the SF_CE0 and LCD_RW signals.

Table 11-2: FPGA Control for StrataFlash and LCD

SF_CE0	LCD_RW	Function
1	1	The FPGA reads from the character LCD.
0	0	The FPGA accesses the StrataFlash PROM

Xilinx XC2C64A CPLD

The Xilinx XC2C64A CoolRunner™-II CPLD controls the five upper StrataFlash address lines, SF_A<24:20> during configuration. The four upper BPI-mode address lines from the FPGA, A<23:20> are not connected. Instead, four FPGA user-I/O pins connect to the StrataFlash PROM upper address lines SF_A<23:0>. See Chapter 16, “XC2C64A CoolRunner-II CPLD” for more information.

The most-significant address line, SF_A<24>, is not physically used on the 16 Mbyte StrataFlash PROM. It is provided for upward migration to a larger StrataFlash PROM in the same package footprint. Likewsie, the SF_A<24> signal is also connected to the FX2_IO<32> signal on the FX2 expansion connector.

SPI Data Line

The least-significant StrataFlash data line, SF_D<0>, is shared with data output signals from serial SPI peripherals, SPI_MISO, and the serial output from the Platform Flash PROM as shown in Table 11-3. To avoid contention, the FPGA application must ensure that only one data source is active at any time.

Table 11-3: Possible Contention on SPI_MISO (SF_D<0>) Data

Condition	Function
FPGA_M2 = Low FPGA_M1 = Low FPGA_M0 = Low INIT_B = High	Platform Flash outputs data on D0.
SF_CE0 = Low SF_OE = Low	StaraFlash outputs data.
AD_CONV = High SPI_SCK	Serial data is clocked out of the A/D converter.

DAC_CS = Low SPI_SCK	DAC outputs previous command in response to SPI_SCK transitions.

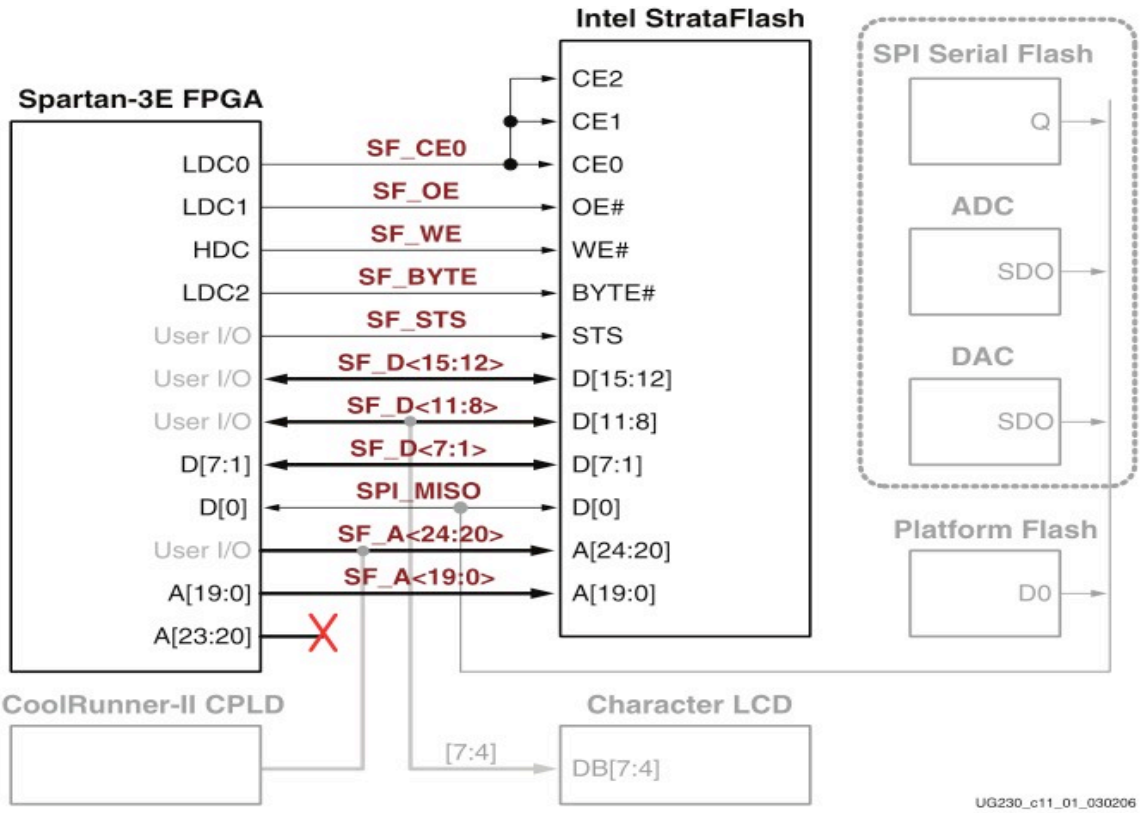

Figure 11-1: **Connections to Intel StrataFlash Flash Memory**

SPI Serial Flash

Shared SPI Bus with Peripherals

After configuration, the SPI Flash configuration pins are available to the application. On the Spartan-3E Starter Kit board, the SPI bus is shared by other SPI-capable peripheral devices, as shown in Figure 12-17. To access the SPI Flash memory after configuration, the FPGA application must disable the other devices on the shared PCI bus. Table 12-3 shows the signal names and disable values for the other devices.

Table 12-3: Disable Other Devices on SPI Bus

Signal	Disabled Device	Disable Value
DAC_CS	Digital-to-Analog Converter (DAC)	1
AMP_CS	Programmable Pre-Amplifier	1
AD_CONV	Anlog-to-Digital Converter (ADC)	0
SF_CE0	StrataFlash Parallel Flash PROM	1
FPGA_INIT_B	Platform Flash PROM	1

Other SPI Flash Control Signals

The M25P16 SPI Flash has two additional control inputs. The active-Low write protect input (W) and the active-Low bus hold input (HLD) are unused and pulled High via an external pull-up resistor.

Variant Select Pins, VS[2:0]

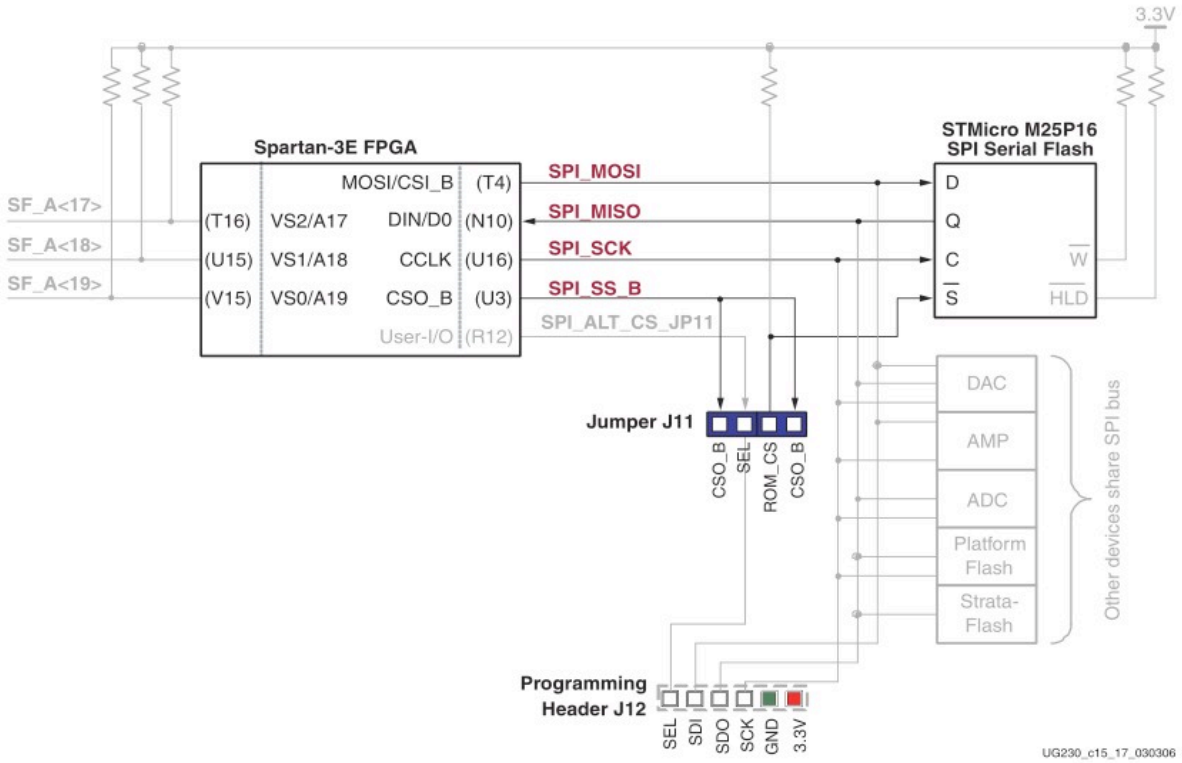

Figure 12-17: **Additional SPI Flash Interface Design Details**

When in SPI configuration mode, the FPGA samples the value on three pins, labeled VS[2:0], to determine which SPI read command to issue to the SPI Flash. For the M25P16 Flash, VS[2:0]=<1:1:1> issues the correct command sequence. The VS[2:0] pins are pulled High externally via pull-up resistors to 3.3V. The VS[2:0] pins are also parallel NOR Flash address lines A[19:17] in the FPGA's BPI configuration mode and these signals also connect to the StrataFlash parallel Flash PROM. After SPI configuration, the VS[2:0] pins become user-programmable I/O pins, allowing full access to the StrataFlash PROM, despite that the FPGA configured from SPI Flash.