DRAM System
Signalling, Timing, Organization

Reference: “Memory Systems: Cache, DRAM, Disk
Bruce Jacob, Spencer Ng, & David Wang
Today's material & any uncredited diagram came from chapters 9 & 10

Signal Integrity

- Increasingly limiting in shrinking processes
  - gets even worse
    - as speeds increase
    - as trace length increases
- Multi-drop wires are a problem
  - very difficult to achieve perfect transmission line behavior in practice
    - Impedance changes with
      - temperature
      - manufacturing variability
      - L & C effects of the neighborhood
      - signal reflections
    - result is signal distortion
      - made worse by noise
        - also a neighborhood problem
- DRAM systems
  - traces are long, and broadcast is the norm
    - intra- and inter-device
Transmission Line Behavior

- **Telegraphers equations**
  - basically a simplified case of Maxwell’s equations
  - lots of PDE’s but key is lumped transmission line
  - typical view is $R$ & $G$ are small - e.g. lossless line
  - position $x$ and time $t$ and hence wave velocity $v$

  $\frac{\partial}{\partial x} V(x, t) = -L \frac{\partial}{\partial t} I(x, t)$

  $\frac{\partial}{\partial x} I(x, t) = -C \frac{\partial}{\partial t} V(x, t)$

- key is that the phase shift of a propagating signal varies with its frequency
- lots of frequency components in real signals
- signal received is not the same as the signal sent

Two Signalling Regimes

- **Depends on the frequency**
  - we try to stay in the RC world
    - high frequency components enter due to reflections

  $Z_0 = \frac{R}{\sqrt{LC}}$

  $Z_0 = \frac{R + j\omega L}{\sqrt{GC}}$

  $Z_0 = \frac{L}{\sqrt{C}}$
Reflection

- Due to mismatched transmission line segments

Non-Terminated Reflection Ladder

\[
\rho (\text{load}) = 1 \\
\rho (\text{source}) = -0.3333
\]

Assume
\[
Z_0 = 100 \, \Omega \\
Z_S = 50 \, \Omega \\
Z_L = \infty \\
V_i = 2 \, V
\]

\[
V_S (initial) = V_i \frac{Z_0}{Z_S + Z_0} = 1.33 \, V
\]
Multi-Drop Bus Complications

• Result
  • as speeds increase
    » #DIMMs per channel decrease
    » delay added by slow rise time and let ringing settle
      • hmm - faster means more delay - huh?
  • socketed DIMM connector adds another discontinuity
    » socket - PCB trace - connector - DIMM trace to DRAM die

Other Complications

• Skew

• Jitter
  • small fluctuations in signal propagation velocity due to
    • temperature, supply voltage, etc

• Inter-Symbol-Interference (ISI)
  • L & C induced cross-talk

• Bottom line
  • lots of practical barriers to increasing signal speed
Termination

- **Key to minimizing reflections**
  - but DRAM needs to be cheap
    - cheap SOJ and TSOP packages
      - large pin C & L's - mismatched to trace impedance
      - OK for low freq - < 200 MHz
    - faster requires smaller pins ==> BGA (DDR) & FBGA (DDR2/3)

- **Another termination issue**
  - Impedance inside vs. outside the package need to be isolated
    - series termination (DDR)
      - damps internal DRAM component reflection effects on the DIMM trace
    - programmable on die parallel termination (DDR2)
      - higher speeds ==> tighter reflection constraints
      - configuration register controls termination resistor switches
      - removes need to time for worst case configurations (max DIMMs)
Termination: Eye Doctor

Voltage Issues

- **Low voltage swing**
  - saves power and potentially improves speed
  - BUT: reduced noise immunity
    - so do differential signalling
    - problem - DRAM’s have to be cheap
      - can’t afford 2x data pins

- **Vref**
  - provide a common voltage reference used by all inputs
    - adv: x+1 < 2x pins for interesting values of x
    - disadv: lose the common mode rejection of differential
DRAM Voltage Standards

- Series stub termination logic
  - SSTL_2 - used for 2.5v DDR parts
  - SSTL-18 - used for 1.8v DDR2 parts
- Similar idea just different standards
  - for SSTL_2, Vref = 1.25v

Rambus Versions

- RSL - Direct RDRAM parts
  - Vref based but with lower swing
- DRSL - full differential, bidirectional, point to point
  - signaling interface must be isolated from core (mats)
  - fast but costly due to additional non-mat interface circuitry
Timing

- Modern DRAM is synchronous
  - clock also a victim of
    » skew, jitter, signal integrity
    » broadcast nature means big L & C components
- 3 clocking regimes
  - global clock
    » slow since timing margin accommodates worst case
  - source synchronous clock forwarding
    » RDRAM and DDR
  - phase or delay compensated clocking
    » PLL or DLL synchronization in newest parts
      - DDR (DLL), XDR (PLL)
- Memory controller gets more complex
  - responsible for timing and command sequence control
    » needs to stay in the center of the eye

Control Addr vs. Data Bus

- Control and Address information is broadcast
  » higher bus load means slower
- Data is pseudo point-to-point
  » memory module knows if it's the addressee
    » others go to Hi-Z connect to data bus
  » key to allowing the DDR scheme to work
  » DDR does complicate things however
    » mem_ctl now needs to deal with 90 degree phase changes
**Column Read & Write in DDRx**

**DRAM Organization**

- **Remember**
  - terminology varies with standard
    - e.g. Rambus vs. JEDEC
  - and even within JEDEC by vendor to a lesser extent
- **In general**
Vendor Channel Variation

DIMMs and DRAMs

<table>
<thead>
<tr>
<th>DRAM chip type</th>
<th>DIMM Stick Type</th>
<th>Bus Clock Rate (MHz)</th>
<th>Memory Clock Rate (MHz)</th>
<th>Channel Bandwidth (GB/s)</th>
<th>non-ECC Channel Width</th>
<th>ECC Channel Width</th>
<th>Prefetch Buffer Width</th>
<th>Vdd</th>
<th>Read Latency Typical (bus cycles)</th>
<th>DIMM pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR-200</td>
<td>PC-1600</td>
<td>100</td>
<td>100</td>
<td>1.6</td>
<td>64</td>
<td>72</td>
<td>2</td>
<td>2.5</td>
<td>2-3</td>
<td>184</td>
</tr>
<tr>
<td>DDR-266</td>
<td>PC-2100</td>
<td>133</td>
<td>133</td>
<td>2.133</td>
<td>64</td>
<td>72</td>
<td>2</td>
<td>2.5</td>
<td>2-3</td>
<td>184</td>
</tr>
<tr>
<td>DDR-333</td>
<td>PC-2700</td>
<td>187</td>
<td>187</td>
<td>2.667</td>
<td>64</td>
<td>72</td>
<td>2</td>
<td>2.5</td>
<td>2-3</td>
<td>184</td>
</tr>
<tr>
<td>DDR-400</td>
<td>PC3200</td>
<td>200</td>
<td>200</td>
<td>3.2</td>
<td>64</td>
<td>72</td>
<td>2</td>
<td>2.5</td>
<td>2-3</td>
<td>184</td>
</tr>
<tr>
<td>DDR2-800</td>
<td>PC2-3200</td>
<td>100</td>
<td>200</td>
<td>3.2</td>
<td>64</td>
<td>72</td>
<td>4</td>
<td>1.8</td>
<td>3-9</td>
<td>240</td>
</tr>
<tr>
<td>DDR2-333</td>
<td>PC2-3200</td>
<td>133</td>
<td>266</td>
<td>4.267</td>
<td>64</td>
<td>72</td>
<td>4</td>
<td>1.8</td>
<td>3-9</td>
<td>240</td>
</tr>
<tr>
<td>DDR2-800</td>
<td>PC3200</td>
<td>187</td>
<td>333</td>
<td>5.333</td>
<td>64</td>
<td>72</td>
<td>4</td>
<td>1.8</td>
<td>3-9</td>
<td>240</td>
</tr>
<tr>
<td>DDR2-800</td>
<td>PC3-6400</td>
<td>200</td>
<td>400</td>
<td>6.4</td>
<td>64</td>
<td>72</td>
<td>4</td>
<td>1.8</td>
<td>3-9</td>
<td>240</td>
</tr>
<tr>
<td>DDR3-880</td>
<td>PC3-6400</td>
<td>100</td>
<td>400</td>
<td>6.4</td>
<td>64</td>
<td>72</td>
<td>8</td>
<td>1.5</td>
<td>?</td>
<td>240</td>
</tr>
<tr>
<td>DDR3-1068</td>
<td>PC3-8500</td>
<td>133</td>
<td>533</td>
<td>8.53</td>
<td>64</td>
<td>72</td>
<td>8</td>
<td>1.5</td>
<td>?</td>
<td>240</td>
</tr>
<tr>
<td>DDR3-1068</td>
<td>PC3-10600</td>
<td>167</td>
<td>667</td>
<td>10.67</td>
<td>64</td>
<td>72</td>
<td>8</td>
<td>1.5</td>
<td>?</td>
<td>240</td>
</tr>
<tr>
<td>DDR3-1600</td>
<td>PC3-17000</td>
<td>200</td>
<td>1068</td>
<td>18.08</td>
<td>64</td>
<td>72</td>
<td>8</td>
<td>1.5</td>
<td>?</td>
<td>240</td>
</tr>
</tbody>
</table>