CS/EE 6710 Digital VLSI Design
Project Proposal
Due Tuesday November 19th, 5:00pm

Write a proposal for the chip your group plans to design for your project. I would guess that you could do this in 3-5 pages, but take the space you need. Because this is a proposal, all the details don't need to be figured out, but I should be able to get a good general idea of what you plan to do by reading the proposal. Part of the reason for writing a proposal is to get you thinking about the details of the project now before you get so far down the project path that it's hard to change course. The proposal should include:

- An overview of the chip you plan to design, along with some details of the design (instruction sets, modes of operation, chip features, etc.)
- A description of the approach you're planning on taking for the design. All Verilog? Mix of synthesized Verilog and custom circuits? On-chip RAM or ROM? Are there cells in your library that were designed specifically to fit with your project? Will your project require new cells that aren't in your library yet?
- A block diagram of the proposed system showing the major system pieces and how they interact (e.g. controllers, datapath components, interface components, etc.)
- A data sheet for the external interface to the chip. How many pins will you need? How will you communicate to and from the chip? What external components is your chip designed to connect to?
- Some thoughts about testing the chip. Will you test by plugging it in to a VGA screen and seeing if everything works? Plugging into the tester? Building a test board? Are there ways of testing some of the system components on their own if the entire chip doesn't work? Think about what internal signals it would be good to see in order to find out what's going on (state machine state bits? ALU controls? RF addresses?)

  Remember that you can only communicate to your chip from the I/O pads that you defined. Make sure that you can test things using those external I/O signals. This might involve taking unused pads and connecting deep-inside-the-chip signals to them so you can see what's going on. Think about the type of things you would like to be able to test, especially if the chip doesn't work completely. You might even go so far as to connect all the chip state into a large shift register (using DFF cells that can also go into shift mode) but that's definitely not required.
- Let me know if you are planning on fabricating your chip. This is not required for the class, but is an option. This isn't a contract – you can change your mind about fabbing later if you like. What is a requirement is that if you fab your chip at least one team member must sign up for CS6712 in the spring. Let me know who that will be.