Proposal

Smart Vision Sensors for Entomologically Inspired Micro Aerial Vehicles

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Introduction

Impressive digital imaging technology has become commonplace in our lives. However, this technology simply captures a "dumb" image that must be processed by complex, relatively power-hungry devices in order to extract meaningful information. Biological systems, on the other hand, can capture and process images in a much more efficient way, and in real time.

Next fall, I will begin work on a series of "smart" sensors that mimic the operation of a fly's vision system. These sensors will be used as part of the design of micro aerial vehicles that can be used for situation assessment, building clearing and data capture in potentially dangerous environments. The intelligence of these sensors will allow the devices to be partially autonomous, ideal for difficult or unstable environments.

Project Description

The universities of California, Utah, Boston, Stanford and Caltech have collaborated to develop teams of micro hovering aerial vehicles (MHAVs) and sub-gram micromechanical flying insects (MFIs) that can perform difficult operations of observation, search and data capture in potentially dangerous situations. These teams will consist of several MFIs that are partially autonomous – able to take-off, stay upright, automatically correct for changing air currents, avoid collisions, and land – and one or more MHAVs with greater intelligence that can send simple tasks to the individual MFIs and coordinate the team.

The University of Utah is responsible for developing lightweight, low power sensors that will capture an image for data acquisition, but also provide information about its environment in order to automatically adjust for dynamic changes and avoid running into walls and other objects. I will be developing these chips with the help of Reid Harrison, who has worked on biological-inspired vision sensors for over eight years.

Personal Contribution

Someone will be needed to focus entirely on the vision sensors and perform the design, layout, testing, and analysis. I will fill this role. I have excelled in circuit classes, including the Analog IC course this semester, where I have won competitions for both smallest design and lowest power design of op-amps, both important aspects of this project. Also, with a computer engineering background, I possess the skills necessary to interface the chip with a microcontroller, design software analysis tools, and test the device in meaningful ways. I will also be required to collaborate with other researchers, so I will be able to contribute my ability of working well with others.

Related Work

Reid Harrison has developed several VLSI circuits that mimic the fly's optical processing behavior. These chips use smart pixels that can detect motion in two directions. Each pixel contains optical sensors as well as associated circuitry to convert the data into two simple analog outputs. One of these indicates the magnitude of movement in the x direction and the other indicates the magnitude of movement in the y

direction. Information from several pixels is then combined in different ways to determine optical flow and rotation, and to detect oncoming collisions. Each pixel outputs information as a differential current. This can easily be added to the data from other pixels by simply tying the desired output wires together.

Project Overview

The first task will be to combine Harrison's existing optical flow sensor onto the same chip as a dense CMOS imager. The CMOS imager will be located in the center of the chip and have a resolution of approximately 64x64 pixels. An array of smart pixels will be located on the periphery on all sides. There will be fewer of these pixels as they take up much more space to process the incoming data.

For the first version of the chip, we will develop a method of outputting all of the data from each pixel for exterior observation and data analysis. This may involve an ADC for the pixel data and a serial interface, or some other method depending on the tools for data capture that are available.

Information from the chip will be displayed and analyzed to determine the accuracy of the sensors and the adequacy of the design.

Specifications for subsequent designs will depend largely on the results from testing the first version of the VLSI design. However, some requirements for these revisions are initially apparent.

First, the output of the system must be adjusted to process the smart pixel data in meaningful ways rather than simply outputting the information for outside observation. The exact nature of the outputs will need to be coordinated with the other university groups to provide meaningful information that can be directly used in flight control.

Also, the current sensors extract information about only one aspect of motion. It may be particularly challenging to obtain simultaneous data on rotation, flow, and collisions from the same sensor.

Testing/Integration

One of the most interesting parts of this project will be to develop a testing strategy that is practical and meaningful. A good portion of time will be devoted to this task. After submitting a design for fabrication and while waiting for the physical chip to be produced and delivered, I will fully implement a testing strategy based on the expected nature of the data extracted from the chip.

It is likely that I will need to interface the sensor with a microcontroller that can process the data into a form easily downloadable onto a general-purpose computer. I will develop specific tools using MATLAB that can interpret, display, and analyze the data in meaningful ways. This will allow complex analysis that will help to determine what should be done on the following revisions of the chip.

Later on, it will be necessary to integrate these vision sensors with the MFI. I will likely travel to Berkeley for sensor testing on the actual MFI.

Specific Tasks

The project can be divided into several distinct tasks. Below is a description of each of the major elements of the project for the first year, developing the first version of the vision chip (Senior Thesis). Where appropriate, I have included risk assessment of the different areas.

Learn Lab Tools

It will be necessary first of all to become familiar with the tools available for design, simulation, and layout of VLSI circuits. The tools available are in a suite known as Tanner Tools. These tools are somewhat similar to the Cadence and Synopsis tools used in ECE 5710 and 5720, but are PC based and somewhat less configurable. They should in fact be easier to use than the Cadence tools I am already familiar with. I foresee little difficulty becoming proficient in these tools.

Research Previous Work

Much of the proposed design, such as the "smart" direction pixels, will be based on existing designs of Reid Harrison. I will need to spend significant amounts of time going over these to make sure I understand them completely so that I can effectively duplicate or modify them as needed. I will likely do much of this research over the summer, but plan on spending time at the beginning of the school year when I have access to the complete designs and specifications.

Preliminary Design and Simulation

Once I have obtained a proficiency with the tools and a good understanding of the design specifications and possibilities, I will begin working on the design of the basic chip. The basic elements of the chip are the high resolution CMOS imager, array of smart pixels, and the network that will add or interpret the information from the pixels.

I will simulate parts of the chip as I go along, making sure that I understand exactly how it works and what parameters affect operation of individual parts. If I run into problems at this point, I will discuss them with Reid Harrison for resolution.

Determine Testing Strategy

It will be necessary to develop a testing strategy that will allow sampling of the data from each smart pixel, as well as outputs from the CMOS imager. At this stage I will determine what specifications will affect the design of the chip, allowing all of this information to be extracted. The outside hardware and exact method of extracting the information will be developed later while waiting for the chip to be fabricated.

Design Modifications

Based on the information from simulation and also the testing strategy that will be determined, as described above, several modifications may be necessary in the design. I will take all of these things into account as I make the final modifications of the design.

VLSI Layout

When the design is complete it will be necessary to layout the circuit for fabrication. This is fairly straightforward, but can be quite time consuming, especially as we are quite concerned with providing a small design that can be integrated onto a sub-gram system.

One potential risk during this phase would be finding that the design is simply larger than is acceptable. It will therefore be very important that I consider the layout, and size of the circuit during the design phase. I perform quick token layouts along the way to check on size during design and avoid this potential hazard.

Submit for fabrication

Sometime toward the middle or end of November, we will submit the chip for fabrication. Designs may be submitted for fabrication only at specific times, so I will have to be aware of the deadlines and plan my schedule accordingly.

Implement Testing Strategy

While waiting for the chip to be fabricated, I will implement the testing strategy that was previously determined. As noted above, this may involve the use of a microcontroller for interpreting serial data and transferring that to a PC for analysis. The exact nature of this task will become more clear once the chip is fully designed.

Develop Analysis Tools

Once the output data has been captured from the device, it will be necessary to analyze it to determine whether the design is adequate or lacking in some way. This information will be helpful in determining what to modify and future versions of the chip.

I will develop tools for analysis in Matlab. These flexible programs will interpret the data obtained from the chip in meaningful ways and will be configurable so that important aspects can be analyzed that may present themselves during the testing phase.

Receive Fabricated Chip

The chip will likely be available sometime in February. The exact date will be determined by when the design is submitted. I plan to be prepared to test the chip immediately as it arrives.

Test Chip and Analyze Performance

Here I will use the testing methodology and analysis tools described above. Aims of analysis will be to determine accuracy of the motion detection, sensitivity to lighter or darker environments, sensitivity to distance, accuracy of the CMOS imager, and other

measurements. I will work closely with Dr. Harrison and other team members to determine what is important to test and what to observe as I analyze the data.

Possible problems during this phase are mainly interfacing issues. If there is a flaw in the testing strategy, it is during this phase that it will become apparent. All possible care will be taken to ensure that the testing strategies are accurate and functional before this phase so that debugging of interfaces is minimized.

Documentation and Thesis

I will thoroughly document each task as I perform it in order to minimize preparations for the thesis paper and presentation in April. Evenso, I hope to have a buffer period in which I can dedicate some time to preparing for my Senior Thesis submittal.

Communication Plan

I will be meeting with Reid Harrison each week to discuss how the project is going and resolve any concerns that may come up with the project. If more communication is necessary, especially as chip submittal deadlines approach, we will meet more regularly.

As the project develops further, I will communicate as needed with members of the team working at other universities to determine interface requirements and physical limitations that may arise.

Schedule and Milestones

The following is taken directly from the Project Schedule and Milestones section of the DoD Proposal for this project. I have included only the section relating to the work on visual sensors that will be performed at the University of Utah. Abbreviations are as follows: version one V1, working paper WP, prototype proto. Y0.5 is 6 months past the start of the project, Y1.0 is 12 months, etc.

Optical Flow, Ocelli, and Visual Sensing (Utah)

Design V1 chip with optical flow and CMOS imager	Y0.5	WP
Benchtop testing of V1 chip	Y1.0	proto, demo
Flight testing of V1 chip (at Berkeley, data collection	Y1.5	WP
Design of V2 sensor chip	Y1.5	WP
V2 sensor for integration with MFI	Y2.0	proto
V3 sensor design with roll/pitch/yaw detection+ocelli	Y2.5	WP
Benchtop testing of V3 chip	Y3.0	proto
V4 sensor design with collision avoidance	Y4.0	proto

I will be working on this project for at least the first two years. A more detailed breakdown of my work for the first year, up to my Senior Thesis, is described below.

Tasks	Sep				Oct				Nov				Dec			
Learn Lab Tools																
Research Previous Work																
Preliminary Design																
Design Simulation																
Determine Testing Strategy																
Design Modifications																
VLSI Layout																
Submit for Fabrication																
Implement Testing Strategy																
Documentation																

Tasks	Jan				Feb				Mar				Apr			
Implement Testing Strategy																
Develop Analysis Tools																
Receive Fabricated Chip																
Test Chip and Analyze Performance																
Prepare for Thesis Presentation																
Present Senior Thesis																
Documentation																

Conclusion

For my Senior Thesis, I will work with Reid Harrison to produce the first in a series of biologically inspired vision sensors to be integrated into micromechanical flying insects. I will design these VLSI sensors based on Harrison's previous work and test the physical chip after it is fabricated. Because of my coursework, abilities, and skill set, I am a good choice for this task. These chips will later be integrated onto MFIs developed as a collaboration between professors and students of several universities.

References

Entomologically Inspired Micro Aerial Vehicles, DoD Technical Proposal, R. Fearing, S. Sastry, M. Dickinson, R. Harrison, C. Tomlin, H. Wang.