



XAPP709 (v1.4) November 18, 2005

DDR SDRAM Controller Using Virtex-4 FPGA Devices

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Summary

This application note describes a 200-MHz DDR SDRAM (JEDEC DDR400, PC3200 standard) controller implemented in a Virtex™-4 XC4VLX25 FF668 -10CES device. This implementation uses direct clocking for data capture and an automatic calibration circuit to adjust delay on the data lines.

DDR SDRAM devices are low-cost, high-density storage resources that are widely available from many memory vendors. This reference design has been developed using DDR400 SDRAM components and DIMMs.

DDR SDRAM Description

The DDR SDRAM specification details are available from JEDEC organization, part of the Electronic Industries Alliance (EIA), at <http://www.jedec.org/>. The DDR SDRAM specifications are published in the JEDEC document, under the reference JESD79C.

DDR SDRAM devices are the silicon memory resource most frequently used in systems today, with applications ranging from consumer products to video systems. DDR SDRAM device frequencies range to 200 MHz or DDR400. DRAM devices are available in component or module configurations.

DDR Controller Commands

Table 1 presents the commands issued by the controller. These commands are passed to the memory using the following control signals:

- Row Address Select ($\overline{\text{RAS}}$)
- Column Address Select ($\overline{\text{CAS}}$)
- Write Enable ($\overline{\text{WE}}$)
- Clock Enable (CKE) (always held High after device configuration)
- Chip Select ($\overline{\text{CS}}$) (always held Low during device operation)

Table 1: DDR SDRAM Commands

Signal No.	Function	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$
1	Load Mode Register	L	L	L
2	Auto Refresh	L	L	H
3	Precharge ⁽¹⁾	L	H	L
4	Select Bank Activate Row	L	H	H
5	Write Command	H	L	L
6	Read Command	H	L	H

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Table 1: DDR SDRAM Commands (Continued)

Signal No.	Function	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$
7	No Operation (NOP)	H	H	H

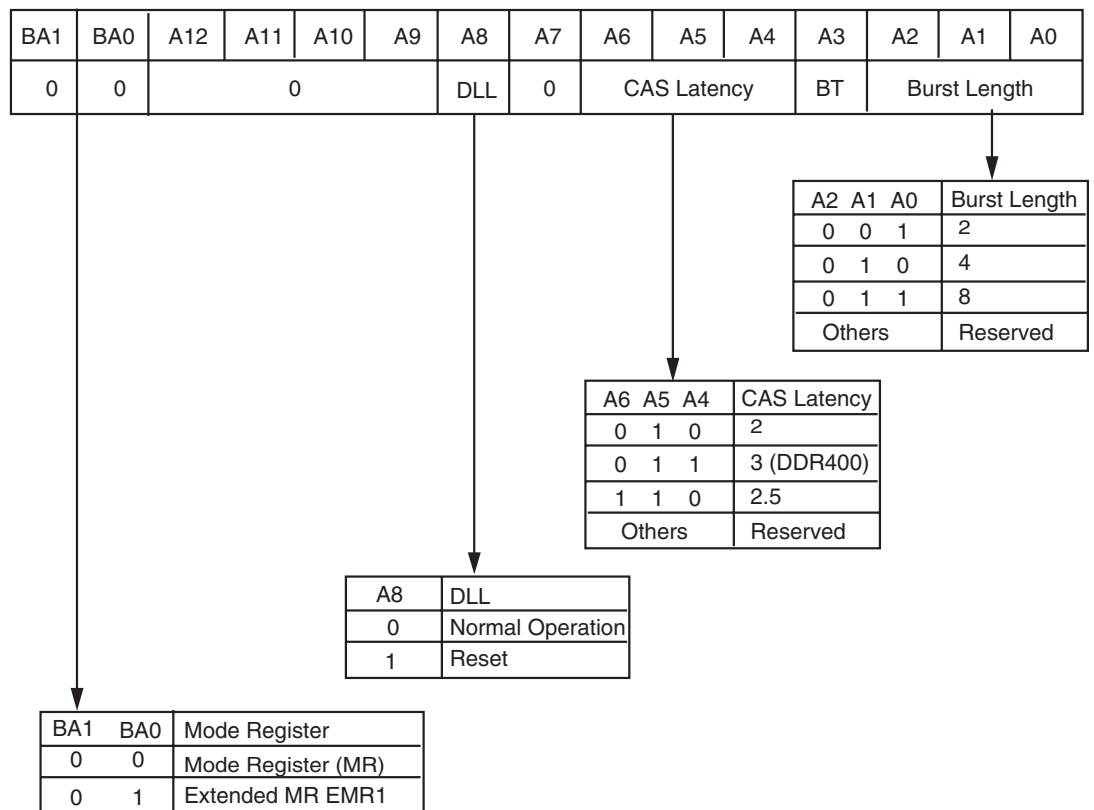
Notes:

1. Address signal A10 is held High during PRECHARGE ALL BANKS and is held Low during single bank precharge.

Command Functions

Mode Register

The Mode register is used to define the specific mode of DDR SDRAM operation, including the selection of burst length, burst type, CAS latency, and operating mode. Figure 1 shows the Mode register features that this controller uses.



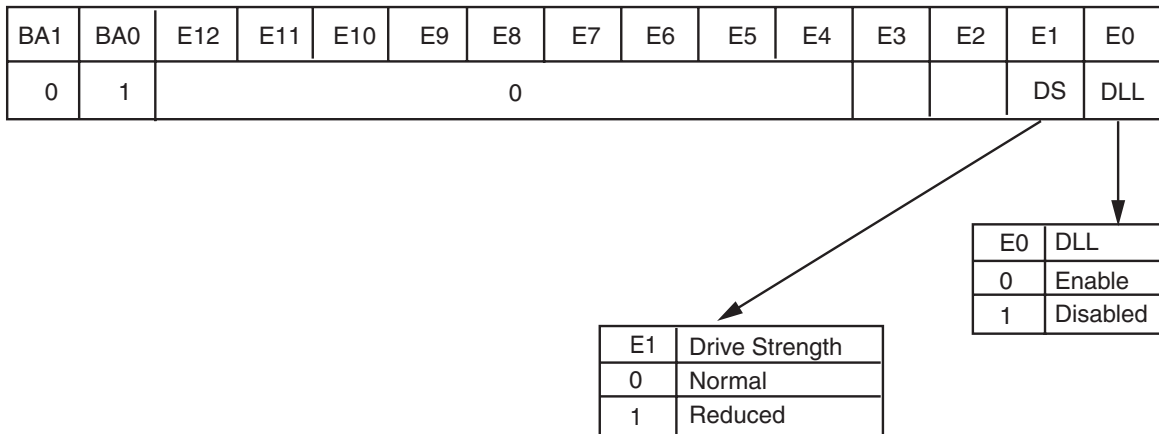
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Figure 1: Mode Register Definition for DDR400

Bank Addresses BA1 and BA0 select the Mode registers. Figure 1 shows the Bank Address bits configuration.

Extended Mode Register

The Extended Mode register controls functions beyond those controlled by the Mode register. These additional functions are DLL enable/disable and output drive strength for DDR SDRAM interfaces shown in Figure 2.

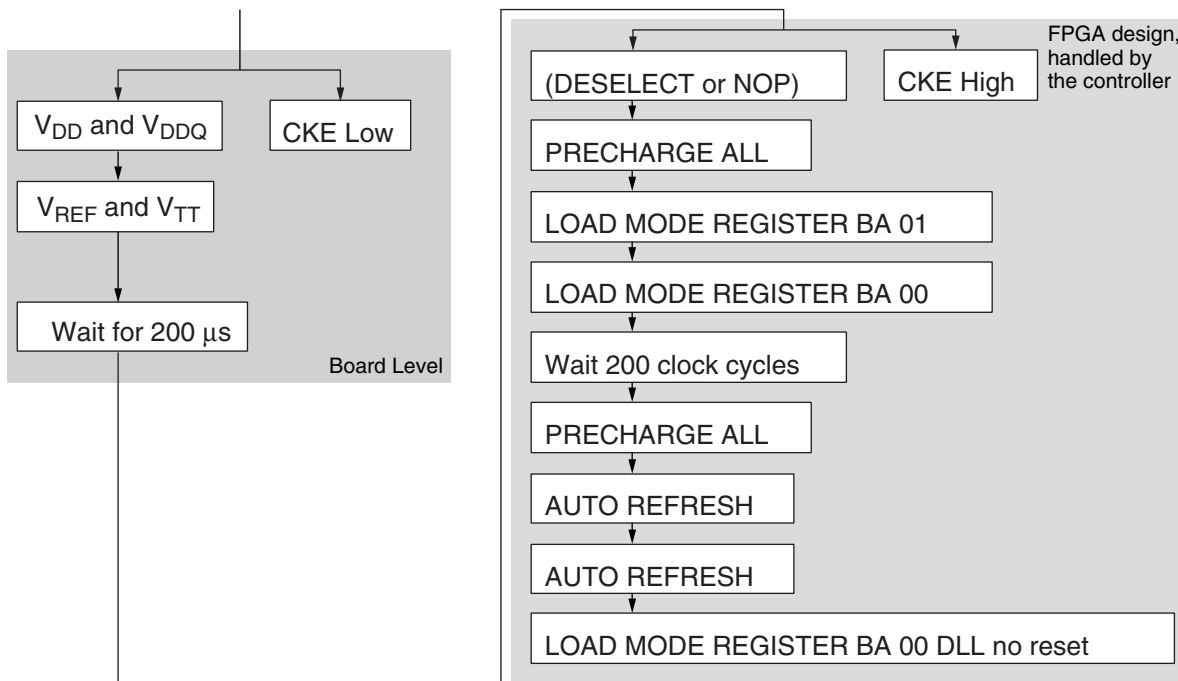


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Figure 2: Extended Mode Register for DDR400

Initialization Sequence

The Initialization Sequence used in the controller state machine follows the DDR SDRAM specifications. The configuration sequence is split in two steps: the first step is handled by the hardware at power up; the second step is handled by the FPGA memory controller design. Figure 3 shows the sequence of commands issued for initialization.



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Figure 3: Initialization Sequence for DDR SDRAM with Virtex-4 Device

After the initialization sequence is complete, the controller issues dummy Read commands to the DDR SDRAM memory device. This process allows the datapath module to select the right number of taps in the Virtex-4 input delay block. The datapath module uses the Data Strobe (DQS) issued by the memory during this dummy Read command period to determine the relationship between the incoming DQS to the internal system clock (CLK0). After the datapath module has determined the right number of delay taps required, a Tap_select_done signal is issued to the controller. The controller then goes into IDLE state.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank. The bank is available for subsequent row activation for a specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are precharged.

AUTO REFRESH Command

DDR devices are required to be refreshed once every 7.8 μ s. The circuit to request auto refresh counters is built inside the controller. The controller uses the DCM's CLKDV output for the refresh counter. This output provides the low frequency clock required for the auto refresh counter. To save on the BUFG that is used by the CLKDV output of the DCM, designers can use the high frequency CLK0 output of the DCM or the CLK/4 output of the DCM (used by the IDELAY Circuit) to clock the refresh counter. If the clock to the auto refresh circuitry is changed, the `max_ref_count` in the `mem_interface_top_parameters_0.v` file needs to be changed accordingly.

The `auto_ref` signal flags the need for a pending AUTO REFRESH command. This signal is held High until the controller issues an AUTO REFRESH command. The controller completes the transactions in a current open bank before issuing the AUTO REFRESH command.

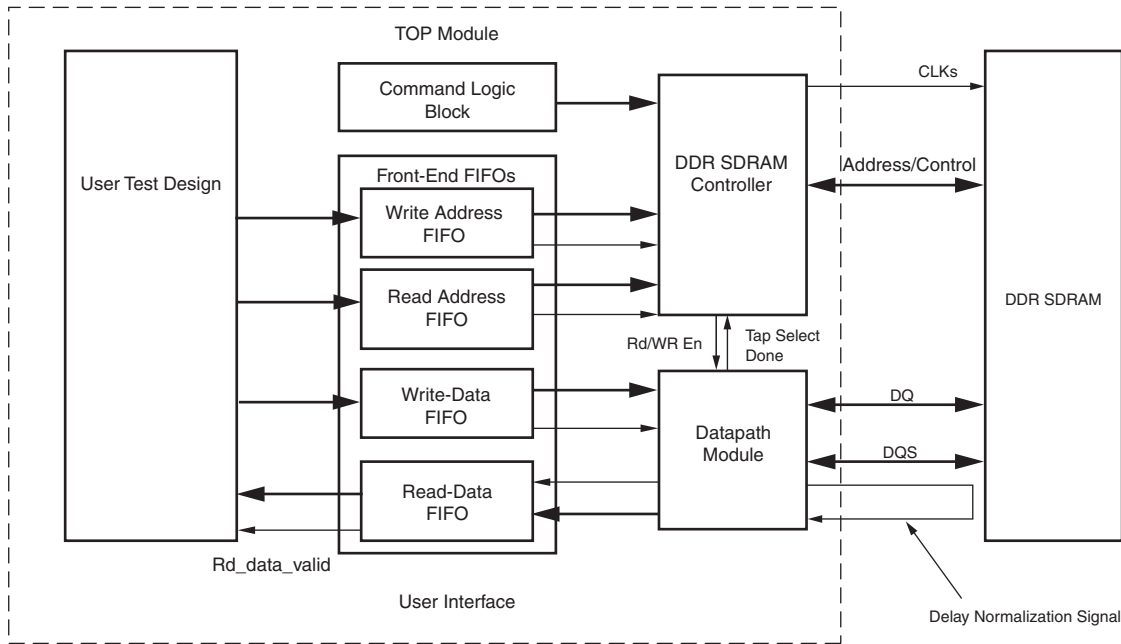
ACTIVE Command

The ACTIVE command activates a row in a bank, allowing any READ or WRITE commands to be issued to a bank in the memory array. After a row has been opened, READ or WRITE commands can be issued to that row, subject to the t_{RCD} specification. When the controller detects an incoming address that refers to a row in a bank other than the currently opened row, the controller issues an address conflict signal. The controller then issues a PRECHARGE command to deactivate the open row and then issues another ACTIVE command to the new row.

READ Command

The READ command is used to initiate a burst read access to an active row. The value on BA0 and BA1 selects the bank address. The address inputs provided on A0 – Ai select the starting column location. After the read burst is over, the row is still available for subsequent access until it is precharged.

Figure 4 shows the case of a READ command with an additive latency of zero. Hence, the Read latency in this case is the same as the CAS latency, which is three in the DDR400 specification.



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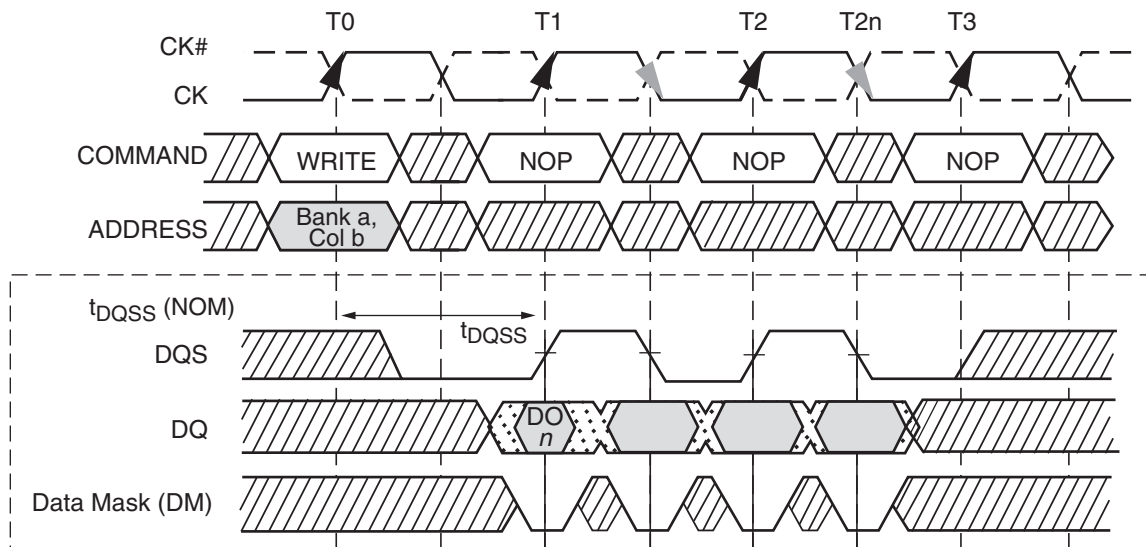
Figure 4: DDR SDRAM Read Access Waveforms

WRITE Command

The WRITE command is used to initiate a burst access to an active row. The value on BA0 and BA1 selects the bank address, while the value on address inputs A0 – Ai selects the starting column location in the active row. The value of Write Latency for DDR SDRAM devices is equal to Read Latency minus one clock cycle.

$$\text{Write Latency} = \text{Read Latency} - 1 = \text{CAS Latency} - 1.$$

Figure 5 shows a Write burst with a Write latency of two. The time between the WRITE command and the first rising edge of the DQS signal is determined by the Write latency.



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Figure 5: DDR SDRAM WRITE Command Waveform

Timing Analysis

The Virtex-4 DDR400 reference design leverages the unique I/O and clocking features of the device to maximize the performance and timing margins.

The physical layer on which the reference design is based uses the Direct Clocking method. It is described in XAPP701: <http://www.xilinx.com/bvdocs/appnotes/xapp701.pdf>.

This section presents an example of timing analysis for the address/control paths, the Write datapath, and the Read (or capture) datapath.

Address/ Control Paths

The address and control signals are synchronized on CLK180 to ensure sufficient set-up and hold margin for the memory device in respect to the clock CLK0.

[Table 2](#) shows an example of the timing analysis for these signals based on a DDR400 interface implemented in a Virtex-4 device using Direct Clocking.

Table 2: Address and Control Signal Timing Analysis

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Description
T_{CLOCK}	5000			Clock period
T_{SETUP}	600	600	0	-
T_{HOLD}	600	-	600	-
$T_{\text{PACKAGE_SKEW}}$	±15	15	15	Package skew
T_{JITTER}	±50	50	50	CLK0 and CLK180 DCM outputs are used to generate DQ and DQS.
$T_{\text{CLOCK_TREE_SKEW}}$	±50	50	50	Small value considered for skew on global clock line because detection of DQS and associated DQ are placed close to each other.
$T_{\text{CLKOUT_PHASE}}$	±140	140	140	Phase offset between any DCM output parameter value, see DS302: Virtex-4 Data Sheet
$T_{\text{PCB_LAYOUT_SKEW}}$	±400	400	400	Skew between data lines and associated strobe on the board
Total Uncertainties	2510	1255	1255	-
Valid Window	2490	1255	3745	-

[Figure 6](#) illustrates the address and control signal timing margins. Because these signals are referenced to CLK180, there is more trailing edge margin than leading edge margin with

respect to the QDR_K clock edge. This allows use of fewer global clock buffers and still provides adequate margin on the leading edge.

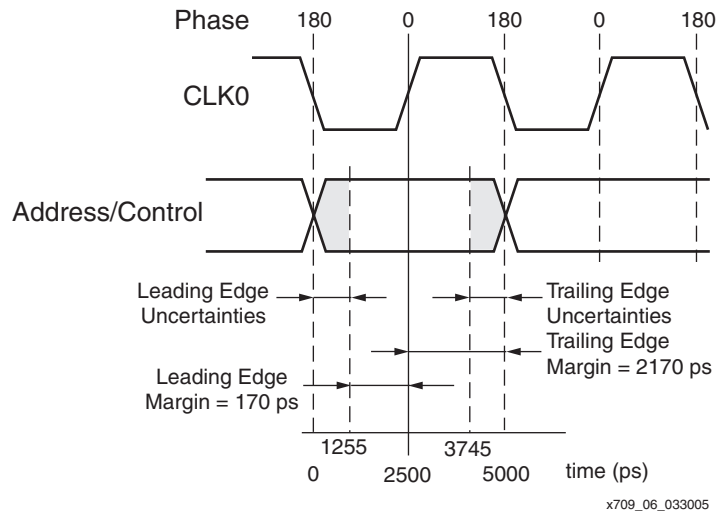


Figure 6: Address and Control Signal Timing Margins

Write Datapath

The Write datapath is also synchronized to CLK270. However, the Write data words are transmitted as DDR values and, therefore, must have adequate setup and hold margins with respect to both the rising edge and falling edges of CLK0.

Accordingly, the timing analysis for the Write datapath, shown in Table 3, incorporates the maximum duty cycle distortion of the memory clocks. This analysis is also for a Virtex-4 device, -10 speed grade.

Table 3: Write Datapath Timing Analysis

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Description
T _{CLOCK}	5000	-	-	Clock period.
T _{DCD}	±250	250	250	Duty cycle distortion of memory clock (5% of clock period).
T _{CLOCK_PHASE}	2250	-	-	Data period is half the clock period with 10% duty cycle distortion subtracted from it.
T _{SETUP}	400	400	0	Setup time from memory data sheet.
T _{HOLD}	400	0	400	Hold time from memory data sheet.
T _{PACKAGE_SKEW}	±15	15	15	Package skew.
T _{JITTER}	±50	50	50	CLK0 and CLK180 DCM outputs are used to generate DQ and DQS.

Table 3: Write Datapath Timing Analysis (Continued)

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Description
T _{CLOCK_SKEW_FPGA}	±50	50	50	Small value considered for skew on global clock line because detection of DQS and associated DQ are placed close to each other.
T _{CLKOUT_PHASE}	±140	140	140	Phase offset between any DCM output parameter value, see the <i>Virtex-4 Data Sheet</i> .
T _{PCB_LAYOUT_SKEW}	±20	20	20	Skew between data lines and associated strobe on the board
Total Uncertainties	1850	925	925	-
Valid Window	650	925	1575	Valid data window

Figure 7 illustrates the Write datapath timing margins. Only the analysis with respect to the rising edge of CLK0 is shown. The analysis with respect to the falling edge of CLK0 is identical.

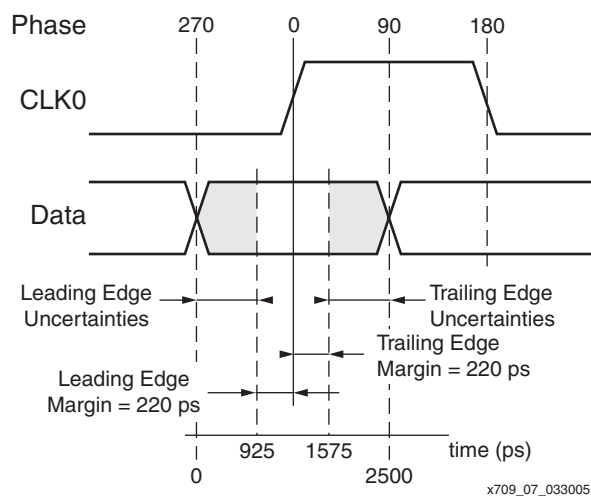


Figure 7: Write Datapath Timing Margins

Read Datapath

The Read datapath values are captured directly into the FPGA clock domain using the previously described direct clocking techniques. Thus, the data capture timing analysis must be performed with respect to CLK0 and consideration must be given to the IDELAY tap delay resolution. In addition, the potential skew between the DQS strobes and the bits of data on the

bus must also be taken into account. Table 4 presents the timing analysis for Read data capture, again assuming a Virtex-4 device, -10 speed grade.

Table 4: Read Datapath Timing Analysis

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Description
T_{CLOCK}	5000	-	-	Clock period
$T_{\text{DCD_MEMORY_DLL}}$	± 150	150	150	Duty cycle distortion from DCM, as specified in the Virtex-4 data sheet, on the signals forwarded to the memory.
$T_{\text{DATA_PERIOD}}$	2350	-	-	Data period is half the clock period with the DCM duty cycle distortion subtracted from the clock period.
$T_{\text{DQS_TO_DQ_SKEW}}$	400	400	0	DQS-to-DQ skew parameter from memory device data sheet.
$T_{\text{HOLD_FACTOR}}$	500	0	500	Hold factor parameter from memory vendor data sheet.
$T_{\text{PACKAGE_SKEW}}$	± 15	15	15	Package skew
T_{IDOCK}	340	340	0	Inherent setup time of the flip-flop in the Virtex-4 device.
T_{IOCKD}	-150	0	-150	Inherent hold time of the flip-flop in the Virtex-4 device.
$T_{\text{IDELAY_MEASURES}}$	± 1 tap	75	75	Evaluation errors: one tap uncertainty per DQS edge (75 ps with 200 MHz reference clock).
T_{JITTER}	± 100	100	100	Clock jitter that indirectly causes strobe jitter as the CLK0 output of the DCM is used.
$T_{\text{CLOCK_SKEW_FPGA}}$	± 50	50	50	Small value considered for skew on global clock line because detection of DQS and associated DQ are placed close to each other.
$T_{\text{PCB_LAYOUT_SKEW}}$	± 50	50	50	Skew between data lines and associated strobe on the board
Total Uncertainties	-	1180	790	Total uncertainties
Valid Data Window	530	1180	1710	

Figure 8 illustrates the Read datapath timing margins.

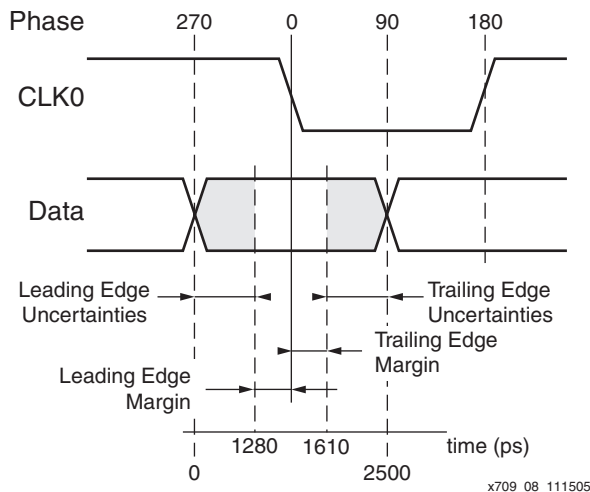


Figure 8: Read Datapath Timing Margins

DDR SDRAM Interface Implementation

This section presents the characteristics of the DDR SDRAM controller and interface, the interface block diagram (Figure 9), and the controller state machine (Figure 10).

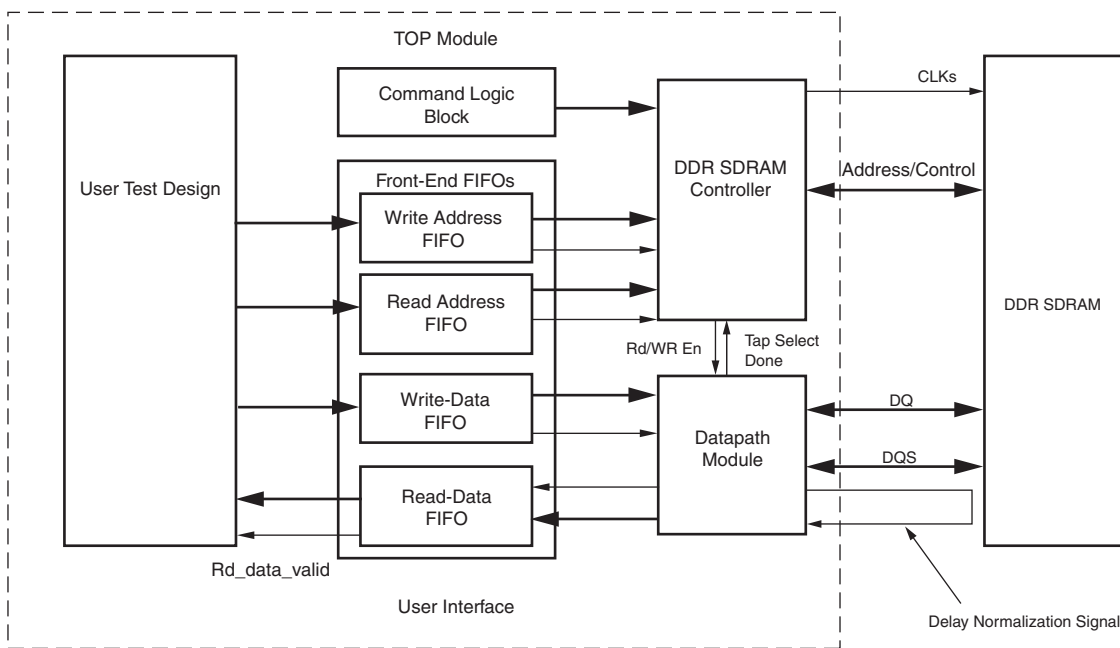


Figure 9: Controller Design Block Diagram

Hardware Test Bench

The hardware test bench provides address and data patterns to test all the design aspects of the DDR SDRAM controller. The user backend includes the following blocks: backend state machine, read data comparator, and a data generator module. The data generation module generates the various address and data patterns that are written to the memory device. The address locations are pre-stored in a block RAM and used here as a Read Only Memory

(ROM). The address values stored have been selected to test accesses to different rows and banks in the DDR SDRAM device. The data pattern generator includes a state machine issuing data patterns. The backend state machine serves as a user design and issues the Write or Read Enable signals to determine which FIFO needs to be accessed by the data generator module.

User Interface

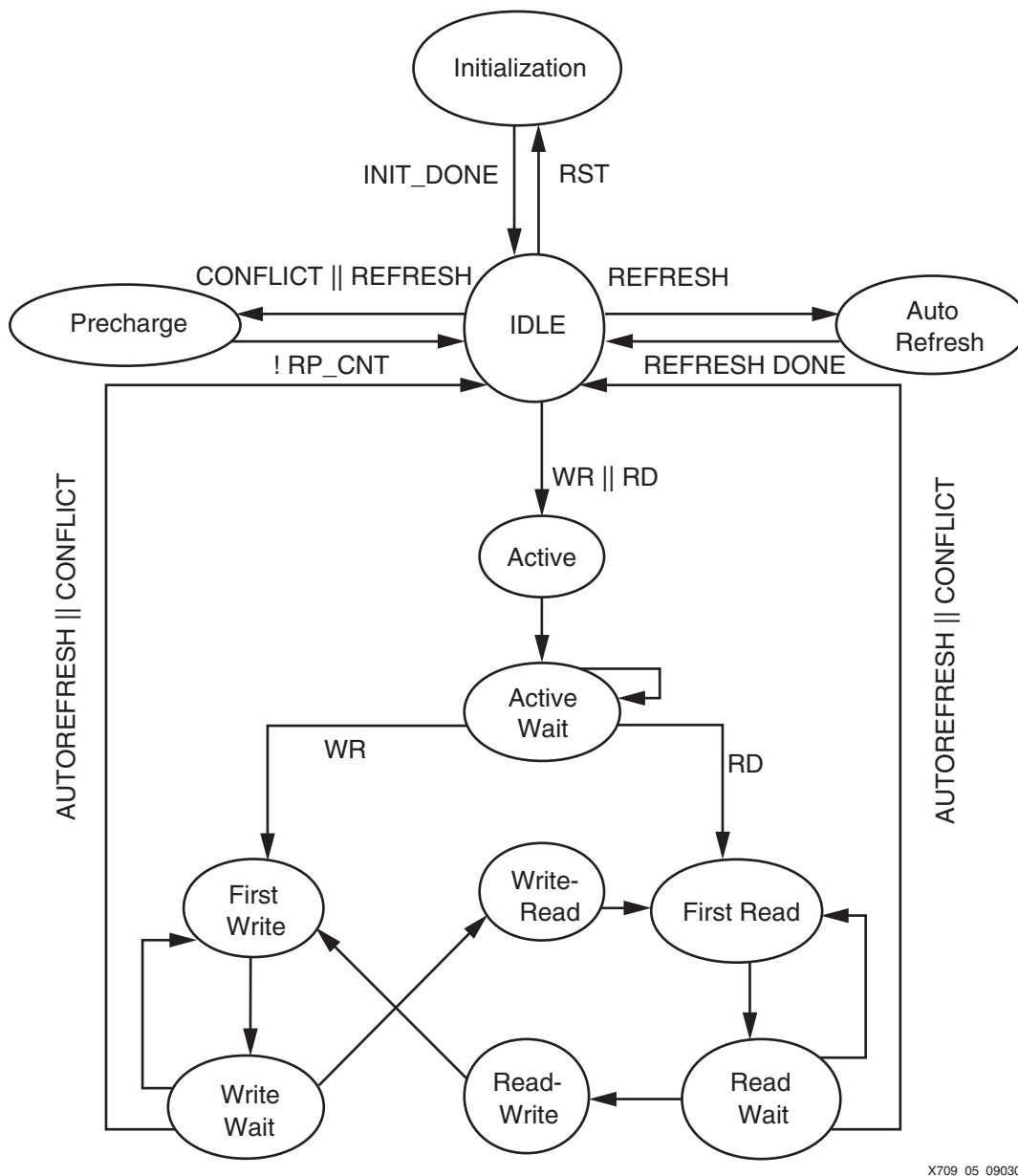
The backend user interface is comprised of four FIFOs, namely the Write Address FIFO, the Write Data FIFO, the Read Address FIFO, and the Read Data FIFO. The first three FIFOs are accessed by the user backend modules, while the Read Data FIFO is accessed by the datapath module to store the captured Read data.

Command Logic Block

The command logic block provides commands to the controller. It can be modified with a designer's command-generation module or replaced with a command FIFO. The command-generation module used in this design generates alternate READ and WRITE commands. The command logic block is a simple state machine that issues the commands to the controller.

DDR SDRAM Controller Interface

Figure 10 presents the state machine of the DDR SDRAM command generation state machine.



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Figure 10: DDR SDRAM Controller State Machine

These are the steps that are followed before the controller issues the commands to the memory:

1. The command logic block generates a WRITE/READ command.
2. The controller issues a Read Enable signal to the WRITE/READ Address FIFO.
3. The controller activates a row in the corresponding bank if all banks have been precharged or compares the bank and row addresses to the already open row and bank address. If there is a conflict, the controller precharges the open bank and then issues an ACTIVE command before moving to the READ/WRITE states.
4. After entering the WRITE state, if the controller sees a READ command, the controller waits for the write_to_read time before issuing the READ command. Similarly, in the READ

state, when the controller sees a WRITE command from the command logic block, the controller waits for the read_to_write time before issuing the WRITE command.

5. The commands are pipelined to synchronize with the Address signals before being issued to the DDR memory.

Reference Design Specifications

The reference design for the DDR SDRAM memory controller using the Direct Clocking Data Capture technique is integrated with the Memory Interface Generator (MIG) tool. This tool has been integrated with the Xilinx CORE Generator™. For the latest version of the design, download the IP update on the Xilinx website at:

http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

The design has been hardware characterized at frequencies higher than 200 MHz. [Table 5](#) provides the reference design specifications.

Table 5: Reference Design Specifications

Parameter	Specifications/Details
Frequency of operation	200 MHz (DDR400 – PC3200)
Virtex-4 device speed grade	10
Device utilization for component design with test bench and ChipScope™	1285 Slices
Number of slices for DIMM interface only	1900 Slices
Number of slices for component interface only	525 Slices
Supported burst modes	4 (2 and 8 with manual modification)
Supported CAS latency	3 (2 and 2.5 with manual modification)
HDL language	Verilog, VHDL
Bus width	Component 16 bits, DIMM 144 bits
Device used for verification for components	Micron MT46V32M16
Device used for verification for DIMMs	Micron MT18VDDF6472AG-40BG4

Design Files

Table 6 lists the reference design files:

Table 6: Design File List With Descriptions for the Verilog Version

Module Name	Description of Each Module
top.v	Top-level module for the DDR controller and Physical Layer.
clk_module.v	Instantiates the DCM_BASE primitive for the memory interface, and the 200 MHz clock for the IDELAYCTRL module. The reference design uses two global clock resources that can be saved by editing the file manually: <ul style="list-style-type: none"> • The first is the counter clock that is generated from the CLKDV output of the DCM. A larger counter can be used to save a clock resource if the timing for the design is met. • The second is the clock for the IDELAY_CTRL module that provides a lower frequency clock for engineering sample parts. The module can use the main interface clock when production devices are used.
data_path.v	Top level for the physical layer. Instantiates the following modules: tap_ctrl, data_tap_inc, idelay_ctrl, idelay_rd_en, v4_dqs_iob, v4_dq_iob, and rd_data_fifo.
data_tap_inc.v	Implements the tap selection controller for data bits associated with a strobe.
idelay_ctrl.v	Instantiates the IDELAYCTRL primitive required when the IDELAY primitive is used in the design.
idelay_rd_en.v	Instantiates the IDELAY primitive and IOB flip-flops for the normalized read enable signal.
tap_ctrl.v	This module detects two transitions of a DQS signal and determines the tap delay required for the associated data bits in order to center them with respect to internal FPGA clock, CLK.
v4_dm_iob.v	Instantiates the IDELAY primitive and IOB flip-flops for the bidirectional data.
v4_dq_iob.v	Instantiates the IDELAY primitive and IOB flip-flops for the bidirectional data.
v4_dqs_iob.v	Instantiates the IDELAY primitive and IOB flip-flops for the bidirectional strobe.
controller.v	<ul style="list-style-type: none"> • Provides the read enable signals to the Write Address, Write Data, and the Read Address FIFOs. • Includes the controller state machine. Supplies the right command signals to the DDR device. AUTO REFRESH commands are generated by the controller taking the Auto Refresh Command Interval into account. • Provides the address signals to the DDR device.
test_bench.v	Synthesizable test bench for the memory interface.
backend_rom.v	Stores the data and address to be written and accessed in the memory array.

Table 6: Design File List With Descriptions for the Verilog Version (Continued)

Module Name	Description of Each Module
cmp_rd_data.v	Generates the error signal in case of bit errors. It compares the read data with expected data value.
user_interface.v	Instantiates the FIFO16 primitive for read data. One FIFO for rising-edge data and the other for falling-edge data.
backend_fifo.v	Instantiates the backend FIFOs for the DDR SDRAM interface. This includes the Write Address and Data FIFOs, and the Read Address and Data FIFOs. The FIFOs are implemented using the Virtex-4 FIFO16 primitives or FIFO made from LUT RAM instances.
Command_logic.v	Constitutes an arbiter for the interface. The user can modify in the module the conditions for read and write accesses for example.
Rd_data_fifo.v	Instantiates the FIFO16 primitive for read data. One FIFO for rising-edge data and the other for falling-edge data.
RAM_8D.v	Instantiates LUT RAMS to build the asynchronous FIFOs. It is configured to clock data on the rising edge of the clock.
parameter.v	Values to be used for the DDR SDRAM reference design at 200 MHz.

Design Hierarchy

Figure 11 summarizes the hierarchy in the reference design in tree view:



Figure 11: Design Hierarchy

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/10/04	1.0	Initial Xilinx release.
11/16/04	1.1	Revised “ACTIVE Command” and “WRITE Command” sections. Added a link to the reference design. Completed Table 6.
04/01/05	1.2	Updated Figure 2, Figure 5, reference design with the results of hardware testing on ML461 platform, “Design Hierarchy”, Table 5, and Table 6. Added “Timing Analysis”.
08/27/05	1.3	Clarified Table 2 and Table 3. Updated reference design with ChipScope files.
11/18/05	1.4	Updated reference design link. See “Reference Design Specifications.” Updated Read Data Timing Analysis (see Table 4) and Figure 11.