

Richard B. Brown

Curriculum Vitae

University of Utah
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Education

Ph.D. E.E.	University of Utah	June 1985
	Dissertation: Multiple-Sensor Chemical Transducer	
M.S.E.E.	Brigham Young University	April 1976
	Thesis: Logic State and Timing Analyzer	
B.S.E.E.	Brigham Young University	April 1976
	Cum Laude, Highest Honors, University Scholar Designation	

Positions at the University of Utah

College of Engineering	Salt Lake City, UT
Distinguished Professor of ECE & KSOC	7/23 –
H. E. Thomas Endowed Dean of Engineering	11/20 – 6/24
Dean of Engineering	7/04 – 6/24
Electrical & Computer Engineering	7/04 –
Professor	
School of Computing	7/04 –
Professor	
Biomedical Engineering	4/05 – 6/25
Adjunct Professor	

Positions at the University of Michigan

Electrical Engineering and Computer Science Department	Ann Arbor, MI
Adjunct Professor	7/04 - 6/11
Interim Chair	7/01 - 5/03
Arthur F. Thurnau Endowed Professor	7/01 - 6/11
Associate Chair representing EE	10/97 - 6/01
Professor	9/97 - 6/04
Associate Professor	9/91 - 8/97
Assistant Professor	9/85 - 8/91

Other Positions

IBM Austin Research Labs Austin, TX
Visiting Scholar, Exploratory VLSI 9/03 - 5/04
Studied low-power circuit techniques in advanced processes while on sabbatical.

Cascade Design Automation Bellevue, WA
Visiting Scientist, Advanced Technology 9/91 - 7/92
Explored advanced electronic design automation concepts and CAD for GaAs technologies while on sabbatical.

Cardinal Computer Division, Cardinal Industries Webb City, MO
Manager Computer Development 1/78 - 9/81
Led team in the development of computers, instrumentation, and printers for process control and electronic weighing applications.

Holman Industries Oakdale, CA
V.P. Engineering 1/76 - 12/77
Designed microcomputer system and dot matrix printers. Directed new product development.

Research

Prof. Brown conducts research in two general areas, solid-state sensors and integrated circuits. In the sensor work, he has enjoyed fruitful collaborative relationships with researchers in chemistry and medicine. Brief summaries of the major accomplishments of his research group follow in related sub-areas ranging from sensors to microprocessors. Ph.D. students' (and post-docs'*) names are listed with the area most closely aligned to their dissertations to aid in identifying the publications related to each topic.

Chemical Sensors: (H. Goldberg, M. Ger, H. Cantor, G.S. Cha*, R. Hower, S. Martin, S. Joo*, T. Strong)

Prof. Brown started working in the area of solid-state liquid chemical sensors in his own Ph.D. research at the University of Utah. Under the direction of Prof. Robert Huber, with Jiri Janata as a very involved member of his committee, he developed a miniature silicon-based chemical sensor array with on-chip electronics. In this project, he developed a junction-isolated NMOS semiconductor process and designed an eight-ion-sensor array using ionophore-doped polymeric membranes, in which the signal from each sensor electrode was buffered by an integrated operational amplifier. This first-of-a-kind smart chemical sensor included digital control circuitry and an analog multiplexer which reduced the number of interface connections needed to seven, which fit on the narrow (1.4 mm) end of the rectangular sensor chip. The junction isolation allowed the sensor chip to be used in solution with only the bond-wire end of the chip encapsulated. The use of integrated electronics improved the signal to noise ratio by more than three orders of magnitude and facilitated the concurrent use of multiple sensors selective to different chemicals. This chip generated all of the data needed to implement chemometrics techniques for reducing errors due to imperfect selectivity of the ionophore-based transducers.

As a faculty member at the University of Michigan, Prof. Brown, and his students continued to solve the fundamental problems in solid-state chemical sensors. They optimized ion-selective membranes for the simple ions based on polyurethane and silicone membrane matrices that had vastly improved biocompatibility and adhesion to the substrate compared to the commonly-used PVC. They developed mass fabrication processes that yielded membranes having precisely controlled dimensions and electrochemical characteristics. They developed a Silicon-on-Insulator (SOI) semiconductor process to give intrinsic encapsulation to these devices that must operate in conductive solution without shorting

high impedance signals to the solution. Throughout the sensor research, novel packaging approaches were developed. The SOI process included a p-i-n photodiode that was used to implement an optically-coupled sensor for detecting alcohol and other non-ionic species. A smart sensor chip was fabricated in this SOI process that included an analog multiplexor, a programmable gain amplifier, a 12-bit analog-to-digital converter, digital control circuitry, and a standard serial interface to a computer – the chip contained most of the instrument as well as multiple sensors.

Solid-state conductivity sensors were developed for quantifying hematocrit levels and the ionic strengths of other fluids. Enzymatically- and immunologically-coupled sensors were demonstrated. Amperometric sensors were developed for detecting and determining the concentrations of neurochemicals (dopamine, serotonin, acetylcholine), heavy metals (arsenic, lead), and any of a host of other molecules that have well-defined redox potentials which lie within the water window. With stripping voltammetry, these sensors were able to detect arsenic and lead at levels as low as 0.3 parts per billion. These sensors were also integrated with electronics, this time using commercially processed CMOS circuits as the substrate; post-processing steps developed in Prof. Brown's lab were employed to form the sensors on top of the circuitry. A model of the full sensor/electronics system was developed to evaluate the noise and optimize the sensor and circuit design. One of the circuits developed and integrated with the sensor was a fully differential potentiostat, which doubled the effective voltage swing available for driving the redox reactions, thereby allowing the electronics to be implemented in modern, fine-featured, low-voltage semiconductor processes. Multiple sensor types were merged onto the same chip to achieve a wide range of sensing capabilities.

With the knowledge and patents generated from this work, Prof. Brown was involved in founding two companies in the year 2000, Sensicore and i-SENS, which commercialized solid-state sensor technology. Sensicore, founded in Ann Arbor, MI, focused on water sensing with a hand-held instrument based upon a single silicon sensor chip that quantified 18 components/parameters of water. More than \$30M of venture capital was invested in the company; it was sold to GE Water and Process Technologies in April of 2008.

i-SENS, headquartered in Seoul, manufactures glucose sensors and point-of-care equipment for monitoring blood gases, electrolytes, and biomarkers related to cardiac function, metabolism (HbA1c), infection, renal disease and maternal health. It has factories in Wonju City, the Incheon Free Economic Zone in Songdo, and in Jiangsu, China. Its CareSens product was the world's first to accurately measure blood glucose in 5 seconds using a blood sample of less than 0.5 uL. In 2019, i-SENS sold more than 1.95M glucometer instruments and 1.65B one-time-use test strips in 80 countries including the US (its largest market). It went public on the KOSDAQ exchange in 2011.

Since being back at the University of Utah, Prof. Brown and his group, with Profs. Cha and Nam from Kwangwoon University, developed several novel reference electrodes that can be miniaturized to sizes comparable to those of the sensors.

Prof. Brown's latest startup company, e-SENS, is located in Research Park next to the University of Utah. e-SENS mates silicon-based solid-state sensors with microfluidics to automate chemical testing. Its first application will be in culinary water treatment and distribution systems. The fully-automated hand-held instrument communicates with an app on the user's smart phone, which manages the calibrations and tests, logs locations, times and test results, and both stores them and transmits them to the cloud or a company server. A sensor module containing calibration and rinse solutions, sensors and microfluidics, is used for a month or 100 tests and then replaced. This system reports 24 components/parameters of clean water in about 15 minutes. Tests are being developed for arsenic, copper and lead, but as important, the instrument reports the Ryznar Stability Index and Langelier Saturation Index, which indicates whether water will deposit calcium carbonate scale in pipes or leach lead from the pipes.

Neural Interfaces: (H. Cantor, T. Strong, R. Franklin, S. Kellis)

Prof. Brown's work in neural sensors started as an effort to apply his group's chemical sensing technology to silicon-based brain probes which, at that time, detected only electrical signals. Communication between neurons happens through both electrical and chemical means, so adding the ability to identify and quantify the neurochemical concentrations in the vicinity of a neuron, along with the electrical spikes, could greatly enhance the understanding of neuron behavior. Their first design was a silicon-based, microfabricated, passive, *in vitro* array organized in a 4 x 4 pattern, in which each sensor used an electrode for sensing the action potential, and with other electrodes formed a voltammetric sensor for monitoring neurochemicals. Five versions of this array were made, with electrode sizes ranging from 2 to 100 μm . The sensor array was packaged in a ceramic integrated circuit pin-grid-array package with lead wires encapsulated, and a small cloning chamber cemented to the sensor chip surface. Human stem cells (hNT cell line from Stratagene) were plated onto the surface over an appropriate matrix, and cultured into neurons. Neurons from this cell line produce spontaneous electrical activity, and secrete acetylcholine and dopamine. Calibration curves for dopamine taken in culture media indicated detection limits for dopamine below 100nM. Neuroelectrical and neurochemical recordings were taken on 24 cell cultures over 75 days. Action potential propagation from neuron to neuron was evident in the data. Electrical spikes and chemical response were correlated in many instances. A cell behavior known as potentiation, in which a neuron fires to prime or activate a particular neural pathway was exhibited in the data; a succeeding pulse causes a larger reaction because of the initial priming. The capture of such events, with multiple action potential spikes in rapid succession followed by a large release of neurotransmitter, highlights the capability of the devices for use in studying the interdependence of neuroelectrical and neurochemical behaviors. This was, to our knowledge, the first case of recording such data without external stimulation. A complete computer model of the sensor's electrochemical behavior was developed for use in optimizing interface electronics. To improve signal fidelity, CMOS potentiostats were integrated into the sensor using the post-processing approach mentioned in the Chemical Sensors section above.

After returning to Utah, Prof. Brown and his students implemented their neurosensors as *in vivo* brain probes that could concurrently detect neurochemical and electrophysiological signals. They studied various materials as they sought a biocompatible reference electrode for neuroprobes, and eventually developed an activated Iridium Oxide Film electrode with excellent characteristics for use in sensing neurochemicals. Silicon needle probes were designed with Pt and IrO_x electrodes on the same shank in appropriate configurations for concurrently measuring local field potentials, action potentials, and neurochemical concentrations. The probes were coated with the perfluorinated ion-exchange resin Nafion to improve selectivity of the platinum sites to more than 100:1 for dopamine over interfering species. The multi-modal probes were implanted in the striatum of urethane-anesthetized rats to examine reciprocal influences of amperometry on neuronal activity, and spatiotemporal characteristics of dopamine effluence vs. local field potential and spike activity following electrical stimulation of the medial forebrain bundle (MFB). The utility of these probes for neuroscience studies was demonstrated as extra-synaptic dopamine overflow in the striatum was correlated with local field potentials and electrical spike activity driven by the frequency and amplitude of electrical stimulation of the MFB. These probes have been made available commercially through NeuroNexus Technologies, Ann Arbor, MI.

Chronic implantation of neural probes is problematic because as the probes move in the soft brain tissue, they see signals from different neurons, necessitating constant retraining of the decoder. Furthermore, biology tries to encapsulate the foreign body, insulating its sensing electrodes from the signals. To achieve better chronic performance of a brain-machine interface, Prof. Brown and his student, Spencer Kellis, in conjunction with neurosurgeon Paul House and Bioengineering faculty member, Bradley Greger, experimented with tiny 40- μm micro-electrocorticographic (ECoG) electrodes placed on the surface of the brain. Experiments were conducted to determine whether non-penetrating, high-density microwire electrodes could provide sufficient information to serve as the interface for decoding motor cortical signals. These electrode arrays were implanted over the motor cortex in epilepsy patients who performed reaching movements with a computer mouse while data were recorded. The

whole array of 16 electrodes fit in the area normally occupied by a single standard ECoG electrode. It was learned that the electrodes are capable of recording predominantly linearly-independent data if placed 2mm or more apart. Signals from cortical columns, sensed by the micro ECoG electrodes, were filtered into frequency ranges, and the amount of power in each band was monitored. Principle component analysis of the filtered and binned data was used to distinguish between the two movements. The gamma band power at 30-40 Hz increased substantially beginning 500 mS before movement in the contralateral direction; movements in the ipsilateral direction corresponded to a general attenuation in power over the gamma band. The algorithm was able to predict with good accuracy which direction the patient was going to move his arm. While the studies to date involved movement of the arm, the inter-electrode spacing was designed to allow for the decoding of individual finger and hand movements, hopefully enabling the dextrous intuitive control of a prosthetic arm and hand. More detailed studies using both hand and arm movement tasks and more sophisticated decode paradigms will be needed to validate the applications of the non-penetrating electrode arrays. The group's latest thrust has been decoding spoken words from micro ECoG signals taken from the surface of the brain in the area associated with control of the face and throat. The group reported the first differentiation of spoken words using non-penetrating electrodes at the Society for Neuroscience meeting in October 2009. They are currently able to differentiate between 10 words. The hope is that this technology will lead to an option for locked-in patients to communicate. Prof. Brown's group also developed a low-power mixed-signal microprocessor to serve as an implanted interface to micro ECoG arrays and for other biomedical interface applications (see below).

Electronic Circuit Clocking: (P. Stetson, A. Drake, F. Gebara, M. McCorquodale, N. Gaskin)

All synchronous digital systems employ a clock to pace the operation of the circuit. In modern integrated circuits, the clock design has a major effect on both the speed and power dissipation of the circuit. Prof. Brown's group has contributed in several ways to improved integrated circuit clocking. In the mid 1990s, as microprocessors became faster than the clocks that could be distributed on printed circuit boards, phase-locked loops, which multiply the clock frequency, became necessary on-chip modules. The group designed CMOS and Complementary Gallium Arsenide (CGaAs) digital phase-locked loops and delay-locked loops that employed current-steering logic and novel low-voltage circuit techniques to achieve the best phase noise results for a given operating voltage reported to that date. This work included a new simulation technique for analyzing phase jitter. As microprocessor clock frequencies continued to rise, there was a need for ever faster phase-locked loops. Prof. Brown's group developed a new class of oscillators based on an efficient NOR-gate interpolator. Oscillator frequencies as high as 4.6 GHz were achieved in a 0.18 μm CMOS process, with a 3X tuning range and rms jitter values as low as 0.87ps. These circuits were incorporated into IBM integrated circuits. The group also experimented with a resonant clock distribution system, the first to use the parasitic wiring and gate capacitance of the clock tree as the resonant capacitance in a monolithic harmonic clock oscillator. A method for characterizing the effects of circuit data flow on jitter in both standard and resonant clocks was developed, including a method of extracting the jitter contribution caused by data from time-domain and frequency-domain stability measurements.

While designing a commercial microprocessor as a consulting project, Prof. Brown learned that the quartz crystal oscillators typically used as the time-base for digital systems sometimes cost more than the microprocessor they support. The idea was conceived to develop an all-silicon clock generator that could be integrated on the microprocessor, replacing the off-chip crystal and passive devices required to implement a crystal oscillator. Prof. Brown and his student, Michael McCorquodale, evaluated a number of options, and settled on a harmonic oscillator with on-chip inductors and capacitors and extensive compensation circuitry for temperature and voltage variation. This introduced an entirely new approach to clocking microprocessors. Instead of starting with a stable lower-frequency clock and scaling it up with a phase-locked loop, they generated a very high frequency clock and divided it down to the desired frequency. The crystal-derived clock is very clean because of the crystal's high Q. The harmonic oscillator's output is not as good in terms of jitter and stability, but just as noise worsens as the square root of the multiplier in a phase-locked loop, it improves as the square root of the divisor in these circuits, yielding a high-quality clock at the desired frequency. The research involved a sacrificial under-etch to

maximize the on-chip inductor's Q with no added masks or processing steps, so the oscillator could be fabricated in standard, advanced CMOS processes. Major contributions included novel analog circuitry to stabilize the frequency over voltage, temperature and device parameters; fast initial tuning techniques; and packaging solutions to avoid humidity sensitivity. Significant contributions were also made in design methodology for mixed technology (digital, analog, RF and MEMS) systems on chips, and a CAD tool called Newton for MEMS device design was licensed by the University to a third party. The resulting all-silicon harmonic oscillator can be integrated onto a microprocessor or other circuit, entirely eliminating the need for a crystal oscillator in many applications. These all-silicon oscillators have the unique characteristic that they reach stability within as little as 20 nS after power is applied, compared to hundreds of μ S for a phase-locked-loop to reach stability. This makes fine-grained power cycling to reduce power dissipation practical, thereby significantly extending battery life in portable or implanted electronics. The clock generators are smaller, lower-power, more robust physically, and lower cost than crystal oscillators or MEMS resonant oscillators.

Prof. Brown and his student founded Mobius Microsystems to commercialize all-silicon harmonic oscillators. Integrated versions of the oscillators were implemented on USB interface chips, and discrete versions were sold as pin-for-pin replacements for motherboard clocks and as bare die to be bonded into a package with the primary IC, forming a system-in-a-package solution that makes the part self-clocked. Monolithic CMOS harmonic oscillators are a disruptive technology that is having broad impact on the electronics industry. Top-tier Silicon Valley VCs invested in the company, which was acquired in January 2010 by IDT (Integrated Device Technology, Inc.). At IDT, the frequency accuracy and jitter were further improved to within 20 ppm over the commercial temperature and voltage range. The Mobius technology was sold as the IDT 3LG Family of CrystalFree Solid-state Oscillators. Electronic Products Magazine gave the 3LG Family of Oscillators its "Product of the Year Award" for offering up to 75% lower power than crystal-based oscillators and the UBM/EEtimes/EDN ACE Awards named the 3LG product its Analog IC Ultimate Product of the Year. Tens of millions of discrete chips and integrated modules were sold/licensed. Prof. Brown's group integrated these silicon clock generators onto the embedded microprocessors that they designed, and they explored new applications for the basic technology, ranging from ultra-wideband radio transmitters to position sensors.

Circuit Design: (K. Wu, P. Parakh, C. Gauthier, K. Das, R. Rao, J. Sivagnaname, M. Guthaus, A. Ghosh)

The design of circuits underpins all of the areas addressed by Prof. Brown's research group, so there is overlap between some of the activities in this and the other sections.

As electronics became ubiquitous, harsh environment applications, such as on jet engines or under the hood of cars grew. Prof. Brown's group and researchers from the GE Corporate Research and Development Center significantly raised the operating temperatures of bulk CMOS circuits by using a thin epi substrate, higher doping levels, and refractory metal interconnect. They increased 300C latchup holding voltage by 4X and holding current by 30X over an equivalent bulk CMOS process. High-temperature design rules were developed that assured latchup-free operation at 200C. A transistor model that accurately represented the space charge at high temperatures (by solving the Poisson's equation and two-carriers' current continuity equations instead of assuming the depletion layer approximation) provided insights into circuit operation at very high temperatures. For example, it became clear that silicon circuits can never operate at high speeds and high temperatures because, in addition to the mobility degradation, the small-signal capacitance equivalent depletion-layer width becomes very small at high temperatures, significantly increasing the parasitic capacitive load.

While microprocessor clock speeds increased during the 1990s at a rate of about 40% per year, off-chip signaling rates improved more slowly, at about 14% per year. Concurrently, the number of transistors on chips increased according to Moore's Law (doubling about every 18 months) but the number of package pins increased at only about 12% per year. Despite the development of more latency-tolerant architectures (multi-level caches, prefetching, stream buffers, etc.), these effects led to a significant bandwidth bottleneck between processor chips and off-chip memory. Prof. Brown's group

developed a switched-current transceiver with an active current mirror receiver that achieved Gb/s/pin operation in a 0.5 μm CMOS process (current technology at that time). This cascoded switched-current signaling architecture was also implemented in CGaAs and compared to Gunning Transceiver Logic, large-buffer voltage signaling, and differential signaling. The switched-current interface was found to be four times more power efficient than similar source-synchronous interfaces. Claude Gauthier, who did this research in his Ph.D., is co-founder and CTO of OmniPhy, a leading provider of interface IP.

Prof. Brown pioneered the use of commercial CAD tools in university courses and research, but when a design automation capability they needed was not available in the commercial tool suites, his group sometimes developed it, always building on top of the best available commercial tools and making the new tools compatible with commercial tool flows. Examples of such contributions were the tools for high-performance gallium arsenide (GaAs) circuits and multichip modules. They developed circuit design techniques and CAD tools that guaranteed process tolerance in the circuits; SRAM compilers that optimize the design for the desired power-delay product; a tool that optimally places modules on a datapath; an automatic block placement tool that minimizes routing congestion; an area-I/O place and route tool for flip-chip packaging; and software that guides engineers through the cost-benefit analysis for nonlinear process scaling. On a sabbatical, Prof. Brown worked with Cascade Design Automation to develop a commercial GaAs circuit compiler that incorporated many of these capabilities. In work that was related to clocking, statistical design, and process parameter variation, his group developed a CMOS clock tree optimizer that correlated both clock and data-path parametric sensitivities to make designs more robust. A quadratic programming heuristic was introduced that was able to realize this improvement without sacrificing deterministic skew. The resulting trees have an average improvement of 16.3% in expected skew with the addition of only 2% to clock power. In a project aimed at making the performance of synthesized circuits approach that of custom circuits, the team developed a logical-effort-based transistor sizing tool, coupled to a cell synthesizer that generated physical, logical and simulation views (years before commercial tools offered this capability), and datapath tiling for wirelength minimization and predictable loads. The on-the-fly library generator enabled studies of circuit performance vs. library size. When the group needed embedded benchmark programs that were not readily available, they developed and published the MiBench suite, which is now widely used in industry and academia for benchmarking embedded processor architectures. According to Google Scholar, the original paper has been cited more than 4,660 times, and there are more than 32,000 references to it on the internet. Prof. Brown's group saw a need for a library of digital and analog circuit modules that university students could use in class and research projects, so they developed the University of Michigan Intellectual Property Source (UMIPS), and populated it with circuits from their own projects. This resource facilitated collaboration and the reuse of circuits, so that designers could focus on the modules that were unique to their projects. Users from around the world have tapped this resource.

Working closely with the IBM Research Labs, Prof. Brown and his students developed circuit techniques for partially-depleted (PD) and fully-depleted (FD) Silicon-on-Insulator (SOI) technologies. Most of this work had a theme of reducing power dissipation at a given circuit speed. Prof. Brown spent a sabbatical focused on low-power circuits in SOI in the Exploratory VLSI group of the IBM Austin Research Laboratory just before moving to the University of Utah. Because of SOI's superior short channel effects and better scalability, device technology has since moved to a form of SOI called FinFET. As semiconductor process dimensions and film thicknesses were scaled, subthreshold source-drain leakage and gate-source leakage increased to the point that the leakage power in ICs threatened to exceed dynamic power dissipation. New gate insulators and other process techniques were important parts of the solution, but good circuit techniques were also critical. Prof. Brown's group developed circuits that mitigate the parasitic bipolar effect and timing uncertainty in PD SOI. They studied and refined multi-threshold CMOS (MTCMOS) for PD SOI, improving the gate delay by as much as 45% and the standby leakage by a factor of eight. Similar techniques were shown to be effective in dynamic logic, as well. Design automation tools were developed to guide the design of SOI circuits and implement the new circuit techniques. An optimal header/footer tapering algorithm was developed for FD SOI; it reduced standby leakage by a factor of 20 over that of conventional MTCMOS. A dynamic logic scheme for FD SOI circuits was developed that reduces leakage power by a factor of 10 to 30 while speeding up the

circuits by 15% over a conventional domino logic scheme. All of the new techniques were evaluated in terms of their effects on power rail bounce. Prof. Brown's group was first to study power-performance trade-offs of SOI circuits taking gate leakage into consideration. CAD tools for efficiently estimating gate leakage were developed, and efficient methods for determining the lowest-leakage data vectors to be applied to static combinational circuits in standby mode were developed. Circuit reorganization schemes were developed for both static and dynamic circuits that reduced gate leakage by 75% and total leakage by 40%. Power dissipation in data buses was reduced through the development of skewed pulse buses, which achieved a 20% reduction in active mode leakage, an order of magnitude reduction in standby leakage, and a delay improvement of 20%. Leakage was studied as a function of process parameter variation, and a model was developed for determining the optimal supply voltage for parametric yield optimization. Analog circuits in SOI, such as a body-compensated current mirror that is stable in the presence of gate leakage, and comparators that employ offset cancellation through body biasing, were also designed, fabricated and tested.

In light of the emergence of SOI technologies and effects that have come with aggressive scaling of electronic devices (short channel non-idealities and leakage), Prof. Brown's group took a fresh look at unipolar logic families, using datapath blocks from their PowerPC-architecture PUMA Processor for realistic evaluations. They showed that pseudo-nMOS circuits could reduce standby leakage current by a factor of five, and that these circuits could be designed closer to the maximum performance point, since the load bias can be easily adjusted to compensate for process parameter variability. They also developed two variants of dynamic logic, controlled-load limited switch dynamic logic (LSDL), and hybrid limited switch dynamic logic, which offer better immunity to noise and charge sharing than basic LSDL. Wide implementations of CL-LSDL were shown to reduce power by as much as 50% over conventional CL-LSDL circuits, and H-LSDL improved delay by 30% over basic CL-LSDL. These logic styles are well-suited for high clock rate, high switching activity circuits such as digital signal processors, memory decoders and datapath circuits, and they can be freely mixed with other logic styles.

Among the greatest challenges in modern semiconductor technologies, where the gate oxide is only a few atoms thick and edge roughness of physical features makes a significant difference in transistor dimensions, is the variability of device parameters. Prof. Brown's group has developed a technique for detecting parameter variation and compensating for it, so that circuits can be designed for the desired operating point, rather than needing to be over-designed to tolerate large parameter variations. Other parameter detection schemes are based purely on a representative circuit's delay; they function properly only if the parameter variations of the p- and n-transistors are shifted in the same direction. The approach developed in Prof. Brown's group uses delay, but also considers rise and fall times of signals in the representative circuit, thereby providing independent information on parametric shifts in the NMOS and PMOS transistors. With this information, the overall circuit speed can be adjusted by tuning the power supply voltage, and the gain for each transistor type can be adjusted independently using substrate bias to drive the operating point back to the desired position. This detection and compensation approach is in fact a low-power circuit technique because it minimizes the power wasted in circuits designed to operate with broad parameter variation, and it balances the gain of the p- and n-transistors, forcing the circuit to the most efficient operating point. This technique for forcing transistors to the optimal operating point may be even more useful in analog circuits than in digital circuits. The approach has also been successfully employed by Prof. Brown's group to monitor PMOS devices for negative bias temperature instability and to compensate for this transistor-aging phenomenon. As in all of the research in Prof. Brown's group, the circuits are not only designed and simulated, but are also fabricated, tested, and demonstrated in realistic applications.

IBM Research Labs hired seven of the Ph.D. graduates of Prof. Brown's group, and many of the circuits described in this section were incorporated in IBM products.

High Performance Microprocessors: (J. Dykstra, A. Chandna, T. Huff, M. Upton, T. Basso, S. Gold)

The late 1980s and early 1990s were times of exploration of various semiconductor technologies for the fabrication of microprocessors. With DARPA funding, Prof. Brown's high-speed circuits group designed three gallium arsenide microprocessors in E/D MESFET technology, three in CMOS, and one in complementary heterostructure-insulated-gate FET technology (CGaAs). Prof. Brown was a proponent of holistic design and multilevel optimization; the research group's activities covered many facets of high-performance processor design, including process technology, circuit design, packaging, CAD tools, architecture, and the architecture's relationship to software compilers. In 1993, they presented at the International Solid-State Circuits Conference, a MIPS-architecture GaAs microprocessor that operated at speeds as high as 200 MHz with 24W power dissipation. That clock speed was exceeded only by an ECL processor presented later at the same conference, which was clocked at 300 MHz, but dissipated 115W. Close working relationships developed between this university group and Vitesse Semiconductor, Motorola, MIPS Computer Systems, Cray Computer, Tera Computer, IBM, Green Hills Software, and Cascade Design Automation. The results of their exploration of very large-scale digital circuits in GaAs influenced technology directions taken by Vitesse and Motorola, and paved the way for Tera Computers to build a GaAs supercomputer.

Prof. Brown's group developed a number of MESFET circuits which demonstrated novel ideas at the gate level (e.g., the patented current-mirror memory cell and power-rail logic); module level (e.g., high-speed modified Ling adder); and microarchitecture level (e.g., decoupled superscalar architecture and partially-decoded instruction cache). They were the first group to implement dynamic circuits in complementary GaAs. They also contributed to advanced packaging technologies for high performance computing (multichip modules, fine-pitch flip-chip gold bonding, and area-array I/O). They optimized the PowerPC microarchitecture for implementation in a small transistor-budget, and demonstrated a radiation-hard CGaAs microprocessor that operated at 86 MHz and 2W. Prof. Brown's research group has been one of only a few at universities that had the capability of prototyping modern microprocessors.

Intel and AMD hired Ph.D. graduates from this group, who contributed to the design of their fastest microprocessors.

Mixed Signal Microprocessors: (K. Kraver, F. Gebara, R. Senger, E. Marsman, N. Gaskin, O. Novak, B. Redd)

Working with colleagues at Michigan, Prof. Brown brought his sensor and integrated circuit research areas together through the design of the MS-8 mixed-signal microprocessor which served as a single-chip interface instrument for the solid-state chemical and physical sensors that he and others developed. The MS-8 included voltage, current and capacitive sensor inputs, an accurate on-chip temperature sensor, an analog multiplexor, bandgap voltage reference, programmable-gain instrumentation amplifier, $\Sigma\Delta$ analog-to-digital converter, a complete 8-bit microprocessor, on-chip memory, a 16x16 multiply 40-bit accumulate MAC for signal processing, a variety of counters/timers, and serial and parallel I/O modules. The microprocessor instruction set and modified Harvard architecture were original to this project and aimed at sensor-interface needs; they included bit test and set instructions, a fast interrupt response with 32 priority levels, and ultra-lite direct memory access. It was fabricated in a 0.35 μm digital process.

Prof. Brown was one of five faculty members, led by Ken Wise, at the University of Michigan, who wrote the proposal for the Michigan Wireless Integrated Microsystems Engineering Research Center. This ERC proposal, focused on microsystems for remote environmental sensor and biomedical implant applications, referenced the MS-8 as evidence that the proposers could implement fully integrated systems. Prof. Brown was the thrust leader for Micropower Circuits in the ERC until he moved to become Dean of Engineering at the University of Utah. He continued to be an active researcher in the Center, participating in weekly administrative meetings (by video conference), industrial advisory board meetings, retreats, and annual reviews, through the ERC's sunset.

Low power circuits were a focus of the ERC, since both of its testbeds required operation on battery power. Four microprocessors were designed in the WIMS series. They share a custom 16-bit RISC architecture with a 3-stage pipeline and windowed register file, on-chip memory, a loop cache, several peripheral communication interfaces, and the all-silicon harmonic oscillator described above. Efficient methods were developed for measuring the energy expended in the execution of each instruction, and a power-aware C compiler that uses this information was developed for the WIMS instruction set architecture by Prof. Scott Mahlke's group at Michigan; feedback from the compiler studies was used to optimize the architecture. The Gen 1 processor, implemented in a 180 nm CMOS technology, was aimed at remote environmental sensing applications. It incorporated a full analog front-end that pushed the limits of low-voltage, low-power analog design in advanced digital processes. The nominal process operating voltage was 1.8 V; to accommodate the voltage change as a single battery cell falls from fully charged to its end-of-life potential, the analog circuits were designed to operate on any voltage between 1.8 V and 900 mV. Weak inversion biasing was used extensively to reduce the need for voltage headroom, to reduce transistor noise and power, and to increase amplifier gain. A second-order $\Sigma\Delta$ modulator was employed in the analog-to-digital converter. When driving a 10 k Ω , 150 pF load, the opamp achieves a DC gain of 80 dB, a unity gain frequency greater than 1.3 MHz, and a phase margin of 60°; the opamp draws a quiescent current of 128 μ A. The sub-1 V $\Sigma\Delta$ modulator is enabled by a dynamically biased pseudo-differential integrator. This integrator supports low-voltage operation by employing the reset-opamp technique, thus avoiding the need for high-swing switches. Correlated double sampling curtails the effects of $1/f$ noise, a more serious problem in fine-featured processes.

Gen 2, also implemented in a 180 nm CMOS process, was designed as an implantable cochlear prosthesis controller. In addition to the processor core, memory and peripherals, it included a digital signal processor block consisting primarily of cascaded 1st, 6th and 4th order infinite impulse response filters that implemented the Continuous Interleaved Sampling Algorithm used to drive the electrodes in cochlear prostheses. To provide the required flexibility for patient fitting, all filter coefficients were made programmable by the processor. This chip included clock gating, the ability to modify the clock speed dynamically, and the ability to employ different clocks in the core and in the DSP. Prof. Brown's group took the lead in implementing the cochlear prosthesis testbed, integrating the Gen 2 processor, application software, and chips designed by other WIMS researchers into a demonstration system.

The Gen 3 processor was designed at the University of Utah and fabricated in a 65 nm CMOS process. It added Direct Memory Access (DMA) instructions and scratchpad memory to the architecture, and was used to study the impact of process scaling on memory power and performance. It included the processor, all-silicon clock generator, memory, and hardware DSP functionality to support brain-computer interfaces. The fully-functional microprocessor core dissipated 350 μ W running at 10 MHz or 10 mW running at 100 MHz.

The final version, Gen 4, of this mixed-signal microprocessor, also developed in a 65 nm CMOS process, was designed to be a low-power implantable microcontroller that could handle applications ranging from solid-state sensor and actuator interfaces to wide-band neural interfaces. In addition to the 16-bit microprocessor core, all-silicon clock generator and other features from Gen 3, this chip includes 32 KB of on-chip SRAM, a battery charger powered by inductively coupled coils, a sleep-mode timer, a programmable-gain analog front end, two $\Sigma\Delta$ analog-to-digital converters, two digital-to-analog converters, and an all-digital ultra-wide-band radio transmitter that can transmit at 200 Mbps at an energy per bit of 19 pJ. The UWB transmitter had the highest pulse frequency and lowest silicon area of any reported transmitter. This microcontroller chip fulfilled the original vision of the WIMS ERC, to build a fully integrated instrument on a chip.

Teaching

New Courses Taught at U of Michigan

<u>Title</u>	<u>Introduced</u>	<u>Taught</u>
EECS317 Solid-State Devices and Digital Electronics	F88	F88, F89 W93, W94, W95

Prof. Brown organized EECS317 to have an integrated-circuit orientation. This course gave all EECS students a good introduction to active devices and large-signal circuits, and prepared them for the VLSI course which followed in the senior year. Large-signal circuit models for diodes and transistors were developed from a physical perspective, and circuit analysis with active devices was introduced using digital circuits. The homework assignments emphasized the complementary use of hand analysis and computer simulation.

EECS427 VLSI Design I	F90	F90, W96, W97
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In 1990, Prof. Brown modified EECS427 so that it was organized around the design of a simple 8-bit CISC microprocessor, the baseline architecture of which was given to students as a starting point for their projects. Working in pairs, they chose an application for their processor and made all design decisions to support this application. Lectures covered topics just in time for students to design the cells which were due each week. This project and general approach to 427 were used through 1995. VLSI Design I was a major design experience before ABET had such a requirement.

In 1996, he had a chance to teach EECS427 again, and renewed and updated it in major ways. The project was changed to a simple 16-bit RISC processor and design teams grew to four members. A number of new CAD capabilities were put into place to reduce design time, to introduce students to important industrial CAD capabilities, and to improve design methodology. At the end of the term, each team had designed and verified their microprocessor.

EECS627 VLSI Design II	W86	W86, W87, W88, W89, W90, W91, F92 F93, F94, F95, F96, F97, F98, F99, W01
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Prof. Brown developed EECS627, the UM advanced integrated circuit design course, in 1986; it had been taught once before, but was a very different course. Students gain maturity in 627 as they are exposed to advanced VLSI topics in lectures, and have a realistic design experience. In '86, he introduced CMOS. In '87, a silicon compiler and other commercial CAD tools were introduced. In '92, he introduced design entry with the hardware-description language, Verilog. This course has continued to change to include current topics in VLSI and the latest CAD capabilities. EECS627 enabled many research projects and did much to improve the reputation of the Department in the area of VLSI.

In 2003, Intel identified the UM VLSI curriculum as the model curriculum, and funded Prof. Brown and several colleagues to document and disseminate the curriculum domestically and internationally.

Short Courses and Workshops

<u>Course</u>	<u>Location</u>	<u>Date</u> <u>Enrollment</u>
Ideal VLSI Curriculum	University of the Philippines, Manila	Aug. 9-10, 2005 18
Gallium Arsenide VLSI (Instructor)	Centre Applied Microelectronics Universidad de Las Palmas Gran Canaria, Spain	Nov. 28-29, 1996 35
GaAs IC Primer Course (Organizer)	1995 GaAs IC Symposium San Diego, CA	Oct. 29, 1995 47
VLSI Digital GaAs Circuit Design 'How to Build a 1 GHz Microprocessor' (Instructor)	Helsinki University of Technology Espoo, Finland	July 4, 1995 28
GaAs IC Primer Course (Instructor)	1994 GaAs IC Symposium Philadelphia, PA	Oct. 16, 1994 37
Device Selection and Performance for High Temperatures (Instructor)	1 st Intl. High Temp. Elect. Conf. Albuquerque, NM	June 16, 1991 145
High-Temperature Electronics Workshop (Chairman)	Ford, GE and UM Ann Arbor, MI	Sep. 28, 1990 16

Contributions to Teaching at U of Michigan

When Prof. Brown arrived at the University of Michigan in 1985, the EECS Department's National Advisory Committee had just published a report which recommended that the Department strengthen the integrated circuit design area (VLSI). He decided to make this a focus of his teaching effort.

Early in his career at UM, Prof. Brown realized that one could not teach proper design methodology with the CAD tools that were available at universities at that time. With the support of the Department and College, he chaired an ad-hoc committee to evaluate and procure new CAD tools, with the vision of replacing the fragmentary collection of software packages used in the Department with a consistent set of tools that would satisfy their instructional and research needs. The University of Michigan pioneered the use of commercial electronic CAD tools in academia as the major vendors accepted his proposals to donate their software to the University. His interaction with these companies helped them to establish university programs which have benefited many other schools. The Department's undergraduate circuit and computer courses were restructured to use the commercial design automation software. These tools have been used throughout the undergraduate and graduate curricula at Michigan, and many universities have used the University of Michigan as a model for updating curricula to include electronic design automation.

Prof. Brown's proposal to add VLSI as a new major area of study for M.S. and Ph.D. students led, with the help of others, to the establishment of a new kernel for graduate students. From both academic and research points of view, VLSI grew into one of the Department's strong areas. Prof. Brown developed both the introductory and advanced VLSI courses at Michigan. These courses are widely known in industry and academia for giving students realistic design experiences which prepare them well for careers in integrated circuit design. Many universities have used the introductory course as a model. In addition to computing resources and CAD tools, students involved in VLSI courses and research need some specialized equipment to facilitate their work. Prof. Brown acquired for the Department plotters which can produce large color plots of chip layouts, an IC tester with 360 high-speed channels, and other test equipment that has enabled many class and research projects.

Prof. Brown organized a VLSI contest, originally founded by Kent Smith at the University of Utah, in which UM students participated for 15 years. It raised interest in VLSI at UM and served to improve UM's VLSI reputation with industrial companies and among peer institutions. Companies with an interest in VLSI donated prizes totaling \$15,000-\$20,000 each year. Judges from the sponsoring companies evaluated the entries from the participating universities. UM students did well in the contest. Mentor Graphics ran a Student VLSI Contest for four years which was patterned after this competition. Here too, UM students typically took the top prizes. In 2000, the Utah/UM contest was merged with a contest sponsored by the Design Automation Conference (DAC); it later became jointly sponsored by the International Solid-State Circuits Conference. The new competition, called the Student Design Contest, gave students national exposure. The winners had their expenses paid to attend DAC and ISSCC, where they presented their designs as posters or in oral sessions, and were honored at awards ceremonies. For the VLSI students, this international contest was like competing in the Rose Bowl. The contest had two categories, conceptual and operational. In the first year of this contest (2000), there were 31 entries from 22 of the top universities throughout the world. UM students took first prize in operational and both first and second prize in conceptual, as well as best paper. In 2001, UM students took first prize in operational and first, second and third prizes in conceptual, as well as best paper. In 2002, UM students won third place in the operational category, first place in the conceptual category, and overall best paper award. In 2003, UM students were awarded first and second prizes in the conceptual category. So ended Prof. Brown's coaching career.

VLSI at the U of Utah

Long before Prof. Brown returned to Utah, faculty at the U of U had modeled their introductory VLSI course after the one he had developed at Michigan. Since his arrival at the U, Prof. Brown has worked with the ECE and Computer Engineering faculty to flesh out the rest of the VLSI curriculum. A new faculty member was hired in the VLSI area, and he established the advanced VLSI course starting with Prof. Brown's notes. Prof. Brown acquired for the University a Verigy 93000 integrated circuit tester that not only facilitated his own students' research, but also the course projects and the research of other faculty members. The VLSI program at the University of Utah has become a strong program with a large number of students enrolled.

Graduate Education

Prof. Brown has graduated 31 Ph.D.s.

Administrative Service

Prof. Brown joined the University of Utah as Dean of Engineering in July 2004. Since that time, he has led the development of a strategic plan for the College that has a vision of raising the quality of teaching, research and service to a level comparable to that of the best engineering schools in the world. Its objectives include growing the research enterprise, positioning the College to become a leader in nanotechnology, assisting faculty in their career development, increasing the amount of technology transfer, nurturing alumni relationships, broadening the Engineering donor base, strengthening the academic experience and climate for students, and improving recognition of the College. The faculty, staff and students have worked together to bring about significant progress in each of these areas; special credit goes to the associate deans, assistant dean, development group, outreach staff and public relations team.

To encourage higher levels of faculty performance, clear, consistent objectives were established, regular feedback was provided, and incentives were put into place. A uniform annual Faculty Activity Report (FAR) was instigated through which faculty members report on their accomplishments in the same categories considered in retention, promotion and tenure (RPT) decisions. The full spectrum of performance data from the FARs is regularly presented to faculty, and is used in informal annual reviews and merit salary decisions. The FAR data, entered through a web interface with much of the information pre-populated, fed directly into the University's Authoritative Database. The College of Engineering pioneered this on-line version, which was then rolled out to the rest of the University. That web-based faculty report led to the Elements model currently used throughout the University. Prof. Brown wrote and had adopted new RPT guidelines that restructured the College RPT Advisory Committee and clearly defined expectations for retention, promotion and tenure. The first electronic RPT casebook files were created in the College of Engineering. This approach was then adopted university wide.

Dean Brown negotiated a financial model for the College that rewards individual investigators, departments and the college for increased research activity. This has been a huge motivation for growing research volume. He worked with the Office of Sponsored Projects to send faculty members electronic announcements of calls for proposals; this has now been implemented university-wide. He organized industry-faculty interactions with local and national companies, which has led to direct research funding and to joint funding from government agencies. Annual Engineering research expenditures grew from \$30M in 2004 to more than \$107M based upon ASEE reporting rules.

The College leveraged its current strengths and further expanded interdisciplinary research through the USTAR initiative. Twenty-two USTAR faculty members affiliated with Engineering were hired, most of them world-class senior faculty. This strategic growth has been in the areas of nanotechnology, microsystems, neural interfaces, biomedical devices, computer imaging, animation, and energy. The senior USTAR hires brought with them a standing in their academic communities that immediately benefited the U's reputation.

The Engineering Initiative, which is aimed at increasing the number of engineering and computer science graduates in Utah, represents a large infusion of funding for the College; these funds have been used almost exclusively to hire new faculty members. The U has organized this state-wide initiative and coordinated the lobbying since its inception; the lobbying is our vehicle for communicating the economic importance of engineering to the legislature and governor. Dean Brown's industrial advisory board, typically company vice-presidents or presidents, are a great support in this effort. This board meets as a full group five times per year. A Technology Initiative Advisory Board, also composed of industry representatives, divides the funding allocated by the legislature among the eight state universities. The College receives an additional \$26.8M in ongoing funds each year and has received \$4.3M in one-time funds through the Engineering Initiative. Private and foundation donations have also been critical to growth and progress in the College.

Closely related to the Engineering Initiative is the College outreach program, which has coordinated as many as 40,000 face-to-face interactions with K-12 students per year. College outreach staff, students, faculty, and alumni visit schools or otherwise interact with prospective students. The

Engineering Ambassadors, a select group of students, are heavily involved in outreach and recruiting. Many students come to campus for events such as Engineering Day, Meet and Inventor Night, Girl Scout Engineering Night, and summer camps.

To stay engaged with the faculty, Dean Brown invited one faculty member twice a month to present his/her research to the dean, associate dean for research, advancement group, and public relations team. The College PR team, composed of a writer, a graphics designer, a web master, videographer, and social media staff member, have increased the amount of media coverage of U of U Engineering research by many times. The College brand is becoming better recognized through print and electronic newsletters, a research report produced annually, and an excellent web site.

A new faculty orientation is conducted each August to help faculty efficiently start in all of their responsibilities. Junior faculty members are assigned a mentor in their own department, and the department chair takes primary responsibility for guiding the junior faculty. Dean Brown also meets with junior faculty individually, and by cohorts twice per year, to discuss all aspects of building a strong academic career. To complement the university-level teaching support, a teaching seminar is conducted for junior faculty members. A few months after the new faculty orientation, a follow-up research seminar is held. Books on being a responsible faculty member are given to each junior faculty member. Prof. Brown organized a committee of senior women faculty from the College of Engineering, the College of Mines and Earth Sciences, and the College of Science to make recommendations related to women faculty and student issues. The College adopted a policy of paying 100% of salary during family leave. He also organized a Dean's Advisory Council for Women, that mentors women faculty and advises the dean on women's issues.

Dean Brown has been an advocate for collaborative relations with industry and for commercialization of university research. After hearing from his Industrial Advisory Board about challenges in university-industry relations, he made this topic the focus of discussions with the Engineering National Advisory Council, a group of about 30 of the College's most successful alumni (and adopted alumni). This group meets twice per year with the deans and department chairs and discusses strategic issues in the college; guest speakers have been governors, senators, the commissioner of higher education, and the university president. A task force from this group wrote a resolution on university-industry relations to Pres. Michael Young that had a large impact on the University. Dean Brown served as co-chair of the search committee that hired the new Director of the Technology Commercialization Office; this hire was the key to an excellent tech transfer climate. IP-related disputes with organizations were resolved and more industry-friendly practices were established in the commercialization office. With the commercialization office, Prof. Brown founded the Tech Titans state-wide entrepreneurial competition. Invention disclosures from Engineering more than doubled to about 100, and College of Engineering faculty have spun out more than 100 companies since 2006.

Dean Brown organized the University of Utah Engineering Alumni Association (EAA) in 2005 with a board that meets regularly and bylaws that provide for rotation of officers and board members. Members of the EAA visit K-12 classrooms as part of the College's outreach program and help with retention by interacting with current engineering students. They are involved in graduate student recruiting and other ways of helping the College. The EAA web site and electronic newsletters have increased College communication with the alumni, as well as communication between alumni.

The student academic experience was strengthened through the organization of an Engineering Honors Program tailored to fit the engineering curriculum. This program includes the freshman E-LEAP experience, an undergraduate research opportunity and a service component, and it builds the honors thesis on the engineering senior project. Whereas only a few engineering students per year graduated with honors before, now engineering students make up about a quarter of all university honors students. Questions about class climate were added to the engineering course evaluations; consistent improvement was shown on the answers to these questions. The Engineering Tutoring Center was established to provide free help to lower-division students, and tutoring is now available in all of the departments, helping with retention on many levels. A new Engineering Math sequence was implemented with a focus on applied mathematics, and with recitation sections and in-class remediation

for students who are weak in some area. Engineering graduates are developing better communications skills through the College's CLEAR program, which has been incorporated into curricula throughout the College. Successful ABET accreditation reviews were held in September 2009, 2015, and 2021.

Dean Brown negotiated international student exchange and/or partnership agreements with a number of the top engineering universities throughout the world: Saarland University, Saarbrücken, Germany; Technische Universität, Berlin, Germany, Shanghai Jiao Tong University, Shanghai, China; Tsinghu University, Beijing, China; Seoul National University, Seoul, Korea; Indian Institute of Technology, Kharagpur, India; and Hong Kong University of Science and Technology, Hong Kong, China; and the University of São Paulo, Brazil.

A non-thesis MS degree was implemented in all departments to facilitate the matriculation of Ph.D. students. A Systems Engineering Certificate, available to students across the College, was established. The Nuclear Engineering Program was reinvigorated and a minor in Nuclear Engineering, available to all Engineering and Science students, was approved. Distance education, which had been successfully delivered to students at ATK (more than 75 graduated with master's degrees), was expanded with a Master of Science degrees and certificates in multiple departments. The Electrical and Computer Engineering Department developed 2+2 BS degree for the U's Songdo Campus. The College implemented an on-line graduate application process, mounted a graduate student recruiting PR campaign, and organized a college-wide graduate visitation day to help departments recruit more highly-qualified graduate students. The result was a significant increase in quality of incoming graduate students.

The College of Engineering and the Business School developed an Engineering Entrepreneurship Certificate at both the undergraduate and graduate levels. It includes courses titled "The Business of Entrepreneurship," "Launching Technology Ventures," "Patent Law and Strategy," and "Emerging Technology & Engineering Entrepreneurship," a technical writing course, and a capstone project or thesis. Joint Engineering MS/MBA degrees are also available to engineering students.

The College of Engineering has grown. In 2004, it graduated 484 students; in 2024 the number was 1,394. As enrollments have grown, student quality has also improved; average ACT scores for our direct-admit students are 31, and average high school GPAs are 3.9. The physical facilities have also improved considerably with the dedication of the 100,000 ft² John E. and Marva M. Warnock Engineering Building in February 2007. The former Engineering and Mines Classroom Building was completely renovated in 2008 and renamed as part of the Warnock Engineering Building, adding another 60,000 sq. ft. A major renovation was done to the Merrill Engineering Building before 2004, but many lab and mechanical renovations have been done since to prepare space for the newly hired faculty. With a \$3.3M lead gift, the Energy and Materials Research Laboratory has been expanded into the Floyd and Jeri Meldrum Civil and Environmental Engineering Building. Dean Brown was intimately involved in the programming, fundraising and design of the \$130M, 200,000 ft² Sorenson Molecular Biotechnology (USTAR) Bldg., which houses the Bioengineering Department, engineering faculty offices and research labs, a vivarium to support biomedical research, a microscopy and surface analysis core facility, and a world-class nanofabrication laboratory. The Rio Tinto Kennecott Mechanical Engineering Building was completely rebuilt and is a showpiece of sustainable renovation. A third phase of this building, the Stephen C. & Lynda M. Jacobsen Tower, opened in 2022.

The School of Computing was endowed and named the Kahlert School of Computing in 2022, and in 2023 a \$50M gift endowed and named the John and Marcia Price College of Engineering and the 250,000 sq. ft. John and Marcia Price Computing and Engineering Building, which had its groundbreaking May 16, 2024, a topping off ceremony September 29, 2025, and will be occupied December 2026.

Grants and Contracts

<u>Dates</u>	<u>Title/Participants</u>	<u>Sponsor</u>	<u>Total Funds</u>
1/86 - 7/87	High-Temp. Solid-State Sensor Technology	Ford SRL	\$131,994
7/87 - 7/91	(grant) (P.I. & Proj. Dir.; Co-P.I., F. L. Terry, EECS)	Ford Fund	\$370,000
9/86 - 4/87	Fabrication Feasibility of Multielectrode Arrays (SBIR consultant to Integrated Microsystems)	NIH	\$50,000
10/86 - 10/91	High-Frequency Microelectronics (Participant; Proj. Dir., George Haddad, EECS)	ARO	\$18,000,000
3/87	Digital Oscilloscope and Plotter (Equipment Grant)	HP	\$27,358
4/87 - 12/92	Integrated Sensors for Water Quality Control (P.I.)	Fleck Controls, Inc.	\$289,084
6/87 - 5/88	Micromachined Pressure Sensor (P.I.)	VP Res. UM	\$15,119
5/89 - 4/90	High-Temperature Electronics (P.I.)	G.E.	\$20,000
9/89 - 7/93	Microbiosensor Arrays (P.I. & Proj. Dir.; Co-P.I.s, M.E. Meyerhoff, Chemistry, and A.R. Midgley, Medicine)	NSF	\$574,696
8/90 - 8/94	GaAs Microcomputer (P.I. and Proj. Dir.; Co-P.I.s, T.N. Mudge, R.J. Lomax, K. Sakallah and W. P. Birmingham)	DARPA	\$2,776,270
7/91 - 11/91	High-Speed Digital Tester (P.I.)	ARO	\$149,202
12/92 - 11/95	Rapid Prototyping and Evaluation of High-Performance Computers (Co-PI with Mudge (Director), Davidson, Hayes, Abraham, Birmingham, Sakallah, and Patt)	NSF	\$804,076

7/92 - 6/97	High-Frequency Microelectronics (Participant; Proj. Dir., George Haddad, EECS) (One student support for 1 yr.)	ARO	\$5,840,400
1/93 - 12/93	Solid State Chemical Sensors (P.I.)	Motorola	\$50,000
2/93	Electrostatic Plotter (P.I. - transferred to gift account)	HP	\$49,900
4/94 - 4/95	Evaluation of Polymer Membrane Based ISMOS-FETS and Characterization of Same with Respect to Manufacturability (P.I.)	Motorola	\$166,667
5/94 - 4/95	High Speed Design Tools (Co-P.I. with Pavlidis (Director), Sakallah, and Katehi)	ARPA	\$566,279
7/94 - 7/95	Planar Sensor Fabrication Feasibility Assessment (Co-P.I. with M. E. Meyerhoff, Chemistry)	Mallinckrodt	\$190,487
7/94	Solid-State Sensors (P.I., Unrestricted Gift)	DuPont	\$10,000
9/94 - 8/98	Design Optimization of a GaAs RISC Microprocessor with Area-Interconnect MCM Packaging (P.I. and Proj. Dir.; Co-P.I.s, T. N. Mudge, R. J. Lomax, and K. Sakallah)	DARPA	\$5,002,705
5/95	Solid-State Sensors (P.I., Unrestricted Gift)	DuPont	\$10,000
7/95 - 6/00	GaAs System Implementation (P.I.)	ARPA	\$243,424
7/95 - 6/96	Solid-State Planar Sensor Technology (Co-P.I. with M. E. Meyerhoff, Chemistry)	Mallinckrodt	\$219,739
7/97 - 7/99	Microprocessor Design Verification (Co-P.I. with Hayes (Director), and Mudge)	DARPA	\$660,390
7/96 - 6/97	Silicon-Based Sensor Array for Whole Blood Analysis (P.I.)	Inst. Labs. (IL)	\$200,281

7/97 - 6/00	Instruction Stream Compression (Co-P.I. with Mudge (Director), and Bird)	DARPA	\$1,183,596
1998	Mixed-Signal Microprocessor	National	\$100,000
1/98 - 12/98	Multi-site Potentio-Amperometric Neural Sensor Array (SBIR with Dr. Hal Cantor of Advanced Sensor Technologies, Inc.)	NIH	\$100,000
1998	Analog Circuit Design	Texas Instruments	\$50,000
1998	Silicon on Insulator Circuits	AMD	\$10,000
6/99 - 5/00	Low Voltage Analog Front End	National Semi.	\$100,000
1/99 -12/99	Low Voltage Analog Design	Texas Instruments	\$100,000
10/99 - 9/00	SOI Circuits	AMD	\$20,000
12/1/99 - 11/30/02	Mass Producible Chemical Sensors and Their Measuring Systems	Kwangwoon Univ., Korea	\$24,000
2/1/00 - 1/31/03	SOI Circuits for Analog, Digital, and Mixed Signal Applications	SRC	\$300,000
8/00 - 7/01	SOI Circuits	AMD	\$25,000
8/00 - 7/01	Mixed-Signal Microprocessor	National Semiconductor	\$50,000
9/00 - 8/05	An ERC in Wireless Integrated Microsystems Kensall D. Wise, Director Richard B. Brown, Thrust Leader	NSF	\$29,447,010 my share \$500,000/yr. for first 5 yrs.
10/00 - 9/01	Undergraduate Mentoring Program	SRC	\$18,000
1/01 - 12/04	Electron-Relay Enabled Immunosensor (Co-P.I. with M.E. Meyerhoff, Chemistry)	State of MI - Life Sciences Proposal	\$769,589

2/01 - 1/02	An Optimal Microbial Control System to Enable Environmental Improvement of Aqueous Fluidic Systems Steven Skerlos, Richard Brown, Katsuo Kurabayashi, Kim Hayes, Alexa Rihana	IESET	\$50,000
9/01 - 8/02	Undergraduate Mentoring Program	SRC	\$12,000
9/01 - 12/01	IBM Faculty Partnership Award: YR 1: An SOI, DTMOS Resonant-clocked Floating-point Unit	IBM	\$25,000
1/02 - 12/02	YR 2: Low-Power SOI Datapath Circuits		\$40,000
1/03 - 12/03	YR 3: Mitigation of CMOS Gate Leakage		\$40,000
1/04 - 12/04	YR 4: Robust Low-Leakage Circuits		\$40,000
1/05 - 12/05	YR 5: Embedded Microcontroller to Improve Power		\$40,000
3/01	9 Workstations with Monitors	Sun Microsystems	\$142,038
9/01 - 9/03	Complex Signal Processing ASIC Designs (P.I.; Co-P.I., Dennis Sylvester)	DARPA - BAE Systems	\$786,496
9/03 - 8/04	Sensors for Monitoring and Diagnostics of Bridges (P.I. Andrzej Nowak, Civil and Environmental Engineering)	ISI: Infrastruc- ture Systems Initiative	\$85,000
2003	Focused Ion Beam Workstation John F. Mansfield (P.I., Materials Science and Engineering, EMAL), R. Brown and others	MRI	
9/03 - 12/04	VLSI Design Curriculum (Richard B. Brown (P.I.), David Blaauw, Michael Flynn, Dennis Sylvester)	Intel Foundation	\$202,173
9/05 - 8/08	SST Integrated Particle Counting and Potentiometric Sensor Array for Water Quality Analysis (P.I.; Co-P.I., Henry White, UofU Chemistry)	NSF	\$299,994
7/05 - 6/06	Feasibility of Measuring Autoantibody	ARUP Lab and	\$15,000
7/06 - 6/07	Interference of Physiologically Active Muscle	Dept. of	\$25,000
7/07 - 8/08	Cells Using a Biological Nanosensor (Co-P.I. with Harry Hill, ARUP Labs)	Pathology-UofU	\$30,256

9/05 - 8/08	Neural Probes for Electrical and Chemical Sensing (sub-contract with U Michigan) (Co-P.I., Richard Brown; P.I., Daryl Kipke)	NIH	\$129,371
9/05 – 8/06	An Engineering Research Center in Wireless Integrated Microsystems (sub-contract with U Michigan)	NSF	\$99,881
9/06 – 8/07			\$90,000
9/07 – 8/08			\$90,000
9/08 – 8/09			\$60,300
9/09 – 8/10			\$30,000
5/09 – 8/09	Student Travel Assistance for the Symposium of NSF 35 Years of Chemical Sensors in 215 th ECS		\$6,000
8/09 – 7/12	Detection and Mitigation of Hazardous Releases in Infrastructure Systems (sub-contract with U Michigan) (Co-P.I. with N. Katapodes, director, and A. Stefanopoulou)	NSF	\$70,114
8/09 – 7/10	IGERT: Nanobiosensors, Nanomaterials, and Microfluidics	NSF	
09-11/13	Coagulation Sensor, (Richard B. Brown; P.I.)	FACTOR 14	\$15,140
09/14 – 08/15	E-Chem Catheter Project, (sub-contract with University of Michigan)	NIH	\$45,644
03/14 – 06/15	Prototype Potentiostats for NO-Release, (Richard B. Brown, P.I.)	University of Cincinnati	\$10,000
01/17 – 12/19	Advanced Thromboresistant/Bactericidal Catheters via Electromodulated NO	NIH UM subaward	\$121,942
05/24 –	Cooperative Research & Development Agreement (CRADA) (H. Kim and V. Srikumar PIs for Semiconductor and AI Tasks)	NSA	

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Michael Leavitt, Richard B. Brown, Jefferson Moss, Carlos Braceras, Andrew Gruber, "What's Past is Prologue: Public Policy Lessons from the Past Quarter Century - Technology Capital," Panel at Salt Lake City, March 18, 2024.

Richard B. Brown, "ROAM – Water Testing in the Palm of Your Hand," Florida Society of Environmental Analysis Spring Meeting, Tavares, FL, May 26, 2021.

Richard B. Brown, "The Utah Story," Arkansas Innovation Council Summit, Little Rock, AR, Feb. 19, 2019.

Richard B. Brown, "International Collaboration in Engineering," Chinese Association for Science and Technology Annual Meeting, Salt Lake City, UT, Dec. 2018.

Richard B. Brown, "A Disruptive Technology for Water Quality Testing," Annual Conference of the American Water Works Association, Las Vegas, NV, June 11-14, 2018.

Richard B. Brown, "The Utah Story," Innovation, Discovery and Commercialization Roundtable, University of Arkansas, Fayetteville, AR, May 14, 2018.

Richard B. Brown and Marilyn Davies, "Utah's Winning Formula for Job Growth," PE Magazine, National Society of Professional Engineers, Nov./Dec. 2017, pp. 14-15.

Richard B. Brown, Ross DeVol, Natalie Shirley, Simon J. Tripp, "Economic Impact of Engineering Education and Research Panel," ASEE Engineering Deans Public Policy Colloquium, Washington, D.C., February 5-7, 2018.

Richard B. Brown, "Economic Benefits of Government Investments in Engineering," Impact of Federal R&D, Engineering Deans Public Policy Colloquium, Washington, D.C., Invited Talk/Keynote, February 7, 2017.

Richard B. Brown, Glenn Prestwich, "Faculty Involvement," 2015 Commercialization Interchange, Session Discussion, University of Utah Technology & Venture Commercialization, Salt Lake City, Utah, October 15, 2015.

Richard B. Brown, "Commercialization Support at the University of Utah," Entrepreneurship and Innovation, Engineering Deans Institute, Kiawah Island, SC. Invited Talk/Keynote, Presented, 04/13/2015.

Richard B. Brown, "Helping Meet the Engineering Needs of Hill Field Air Force Base," Invited Talk, Hill Field Management Awards Ceremony, Hill Field Air Force Base, Layton, Utah, March 4, 2015.

Ian R. Harvey, Florian Solzbacher, Bruce Gale, Thomas Parks, Richard Brown, "USTAR/U of U/COE Partnerships to Spur R&D in micro/nano Materials & Systems," COMS / NanoUtah, Salt Lake City, Utah, October 15, 2014.

Richard B. Brown, "The College of Engineering at the University of Utah," Invited talk, University of Utah, Department of Electrical and Computer Engineering, September 29, 2014.

Richard B. Brown, "Instrumenting the Human Body," Seminar presentation jointly sponsored by Michigan Technological University's College of Engineering and the Departments of Bio-medical

Engineering and Electrical and Computer Engineering. Michigan Technological University, Houghton, Michigan, September 22, 2014.

Richard B. Brown, "Growing Engineering for Defense," Invited talk, Society of American Military Engineers, 2014 Annual Scholarship Banquet, Great Basin Post, Hill Field Air Force Base, Layton, Utah, February 12, 2014.

Richard B. Brown, "University of Utah College of Engineering," Invited talk, WECEDHA Meeting, Salt Lake City UT, September 20, 2013.

Richard B. Brown, panel member, "Partnering with Your Dean," Computing Research Association Conference, Snowbird UT, July 22-24, 2012.

Richard B. Brown, panel member, "Creating a Culture of Entrepreneurship among the Faculty," 2012 Engineering Deans Institute, Engineering: Transcending Boundaries, Kauai, HI, April 15-18, 2012.

Richard B. Brown, panel member, "Engineering Education and Research, "How Engineering Colleges Help the U.S. Compete," A Congressional Luncheon Briefing, 2012 Engineering Dean's Council Public Policy Colloquium, Washington, DC, February 8, 2012.

Richard B. Brown, "A Vision for the College of Engineering," Guest speaker, ECE Graduate Seminar, University of Utah, Sept. 23, 2011.

Richard B. Brown, "Engineering a Healthier World: *Helping the dumb to speak, the lame to walk, and the blind to see*," BYU-Idaho University Forum, Rexburg ID, Nov. 18, 2010.

Richard B. Brown, "ECE as a Career in the 21st Century," Honored Distinguished Alumnus talk, Brigham Young University, Provo UT, Oct. 14, 2010.

Richard B. Brown, panel member, "Managing Up – Partnering with your Dean," Computing Research Association Conference, Snowbird UT, July 18-20, 2010.

Richard B. Brown, Keynote talk, "Engineering as a Career in the 21st Century," Energy Solutions Scholarship Banquet, Salt Lake City UT, May 15, 2010.

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Richard B. Brown, "Interfacing to the Brain with Electrochemical Sensors," Lecture Series for the College of Technology and Computing, Utah Valley University, Orem UT, April 2, 2009.

Richard B. Brown, "Silicon Electrochemical Neurosensors," Global Management of Technology Conference 2008, Seoul, Korea, Sept. 25, 2008, slides pp. 189-210.

Richard B. Brown, "Silicon Electrochemical Neurosensors," Korea Technology Industry Co., Technology Research Center, Seoul, Korea, Sept. 26, 2008.

Richard B. Brown, "Electrochemical Neurosensor Systems," seminar at Georgia Institute of Technology, Atlanta GA, May 27, 2008.

Richard B. Brown, "Sensor Interface Electronics," Iowa State University, Ames IA, Nov. 17, 2007.

Richard B. Brown, "Silicon Electrochemical Neurosensor Arrays," University of Puerto Rico, Mayaguez Campus, San Juan, Puerto Rico, April 27, 2007.

M.D. Johnson, M.D. Gibson, L.G. Salas, R.K. Franklin, R.B. Brown, D.R. Kipke, "Spatiotemporal Neurochemical and Electrophysiological Recordings in Rodents," Neural Interface Workshop, Bethesda MD, Aug. 2006.

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Richard B. Brown, panel member, "Mixed-Signal Analog/Digital Circuit and System Design Issued in Scaled Technologies Beyond 65nm," IEEE International 2005 SOI Conference, Honolulu HI, Oct. 2-6, 2005.

Jayakumaran Sivagnaname, Hung Ngo, Kevin Nowka, Robert Montoye, Richard B. Brown, "Study of Wide LSDL Circuit Implementations," IBM Austin Center for Advanced Studies Conference, Austin TX, Feb. 24-25, 2005.

Robert M. Senger, Eric D. Marsman, Richard B. Brown, "Methodology for Instruction Level Power Estimation in Pipelined Microsystems," IBM Austin Center for Advanced Studies Conference, Austin TX, Feb. 24-25, 2005.

Richard B. Brown, "Low-Power Systems-On-Chips," IBM T.J. Watson Research Labs, Yorktown NY, Nov. 17, 2004.

Richard B. Brown, Dennis Sylvester, Michael Flynn, David Blaauw (2004, June 21), VLSI Course Materials [Online]. Available: <http://www.intel.com/education/highered/VLSI.htm>

R.M. Senger, E.D. Marsman, M.S. McCorquodale, F.H. Gebara, K.L. Kraver, M.R. Guthaus, R.B. Brown, "A 16-Bit Mixed-Signal Microsystem with Integrated CMOS-MEMS Clock Reference," invited poster presentation at IEEE International Solid-State Circuits Conference (ISSCC), San Francisco CA, Feb. 15-19, 2004

Richard B. Brown, "Digital, Analog, MEMS Systems-on Chips," Rice University, Houston TX, April 15, 2004.

Richard B. Brown, "Engineering in the 21st Century," BYU Engineering Week, Provo UT, Feb. 27, 2004.

Rahul M. Rao, Richard B. Brown, Kevin Nowka, Jeffrey L. Burns, "Analysis and Mitigation of CMOS Gate Leakage," *Proceedings of the Fifth Annual Austin Center for Advanced Studies Conference*, Austin TX, Feb. 19-20, 2004, pp. 7-11.

Alan J. Drake, Richard B. Brown, "Performance Impact of Gate-Body Signal Phase on DTMOS Inverters," *Proceedings of the Fifth Annual Austin Center for Advanced Studies Conference*, Austin TX, Feb. 19-20, 2004, pp. 35-38.

Richard B. Brown, "Digital, Analog, MEMS Systems-on-Chips," The University of Texas at Austin VLSI Seminar Series, Austin TX, Dec. 3, 2003.

Michael S. McCorquodale, Richard B. Brown, "Monolithic and Top-Down Clock Synthesis with Micromachined RF Reference," *IFIP VLSI-SoC International Conference*, Ph.D. Forum, Darmstadt, Germany, Dec.1-3, 2003.

Richard B. Brown, "Low-Power Mixed-Signal Microcontrollers for Solid-State Sensor Applications," IBM Austin Research Laboratory, Austin TX, Nov. 7, 2003.

Richard B. Brown, "AMS Low Power Microcontrollers," Sept. 13, 2003, at Computer-Aided Network Design Committee workshop (CANDE 2003).

Wei Zhang, Daniel Burke, Hairong Zhang, Sung Choi, Youngmi Lee, Richard Brown, Mark E. Meyerhoff, "Electron-Relay Enabled Immunosensors using Magnetic Microspheres," Michigan Life Sciences Corridor Biotechnology Conference, Novi MI, April 8, 2003.

Alan J. Drake, Richard B. Brown, "Saving Clock Power Using Resonant Clock Generation," Proceedings of the Fourth Annual Austin Center for Advanced Studies Conference, Austin TX, Late News pp. 1-4, Feb. 21, 2003.

Jay Sivagnaname, Rahul Rao, Richard B. Brown, "Dual Issue PowerPC FXU Processor," First Prize in the Design Contest, *16th International Conference on VLSI Design (VLSI DESIGN 2003)*, New Delhi, India, Jan. 4-8, 2003.

S. J. Pace, R. Brown, "Sensor Micro-Arrays Offer Complete Testing Solutions," *Proceedings: The 7th International Conference on the Commercialization of Micro and Nano Systems (COMS 2002)*, Ypsilanti MI, pp. 483-488, Sept. 8-12, 2002.

Steven M. Martin, Roy H. Olsson III, Richard B. Brown, "A Microsystem for Near-Patient Accelerated Clotting Time Blood Tests," First Prize Conceptual Category and Best Paper in the Student Design Contest, *39th Design Automation Conference*, New Orleans LA, June 10-14, 2002.

Richard B. Brown, "Low-Power Mixed-Signal Microcontrollers," Workshop on Low-Power Circuits, Arlington VA, Oct. 11-12, 2001.

Richard B. Brown, "Solid-State Liquid Chemical Sensor Testing Issues," *International Test Conference 2000*, Atlantic City NJ, pp. 1135, Oct. 1-6, 2000.

Richard B. Brown, Spencer M. Gold, Phiroze N. Parakh, Todd D. Basso, "An Evaluation of Complementary GaAs Technology for Microprocessor Applications," *Workshop on Complementary Heterostructure FETs*, Albuquerque NM, Nov. 18-19, 1996.

Marie Meyer, Steve Baier, Richard B. Brown, "Digital GaAs," *Compound Semiconductor* (Magazine), pp. 26-32, September/October 1996.

R. B. Brown, "System Optimization," ARPA EPI (Electronics Packaging and Interconnect) Conference, Arlington VA, Feb. 27-March 3, 1995.

Richard B. Brown, "Biosensors," American Society of Mechanical Engineers Winter Annual Meeting, Dallas TX, Nov. 25-30, 1991.

Richard B. Brown, Kou-Cheng Wu, Mario Ghezzi, Dale M. Brown, "High Temperature Microelectronics for Smart Sensors," Instrument Society of America, Symposium on Innovation in Measurement Science, Aug. 2-5, 1988.

Richard B. Brown, "State-of-the-Art of High Temperature Electronics," GE Aircraft Controls Conference, June 27-28, 1988.

R. B. Brown, "Integration of Electronics with Solid-State Biosensors," Gordon Research Conference on Applied and Environmental Microbiology, July 26-31, 1987.

T. Shimei, R. B. Brown, H. Wang, "Coupling a Multiple Micro-Biosensor with a Process Monitor for On-Line Process Monitoring," Recent Advances in Biotechnology Symposium, June 16-17, 1987.

R. B. Brown, "Integrated Microsensors," Recent Advances in Biotechnology Symposium, July 10- 11, 1986.

R. B. Brown, "An Integrated Chemical Transducer Array," *WESCON '85 Professional Papers*, 27:5, San Francisco CA, pp. 1-8, Nov. 19-22, 1985.

Books

- R. B. Brown, *An Integrated Multiple-Sensor Chemical Transducer*, Ph.D. Dissertation, University of Utah, June 1985.
- R. B. Brown, *A Digital Memory Scope for Logic System Analysis*, MS Thesis, Brigham Young University, April 1976.

Chapters in Books

- Robert Franklin, Steven Martin, Timothy D. Strong, and Richard B. Brown, "Chemical and Biological Systems: Chemical Sensing for Liquids," in *Comprehensive Microsystems 2nd Edition*, Y. B. Gianchandani, P. R. Selvaganapathy (ed.) Oxford: Elsevier Ltd, May 2025.
- Robert Franklin, Steven Martin, Timothy D. Strong, and Richard B. Brown, "Chemical Sensors," in Reference Module in Materials Science and Materials Engineering: Elsevier Ltd, 2015.
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- Richard B. Brown and Koucheng Wu, "Scaling CMOS Design Rules for High-Temperature Operation," in *High-Temperature Electronics*, Randall K. Kirschman, Ed. IEEE Press, New York, 1999, pp. 278- 282.
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- Richard B. Brown and Edward T. Zellers, "Environmental Monitoring," Chapter 20 in *Sensors: A Comprehensive Survey, Volume 1: Fundamentals and General Aspects*, W. Göpel, J. Hesse, J. N. Zemel, Eds., W. H. Ko and T. Grandke, Volume Eds., VCH Publishing Co., West Germany, 1989, pp. 529- 554.

Book Reviews

- Thomas DeMassa and Zack Ciccone, *Digital Integrated Circuits*, John Wiley Sons, Inc.
- David Hodges and Horace Jackson, *Analysis and Design of Digital Integrated Circuits*, 2nd Ed., McGraw Hill.
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- Richard B. Brown, *Research Agenda Proposal for High Temperature Electronics*, NSF, Nov. 1988, pp. 1-19.

Service

Committee Assignments at U of Utah

<u>Committee</u>	<u>Position</u>	<u>Date</u>
Tech. Transfer Office Director Search Com.	Co-Chair	8/04 – 5/05
CoE Industrial Advisory Board	Ex Officio Member	7/04 –6/24
CoE Engineering National Advisory Com.	Ex Officio Member	7/04 –
CoE Executive Committee	Chair	7/04 –6/24
Utah Science Technology and Research (USTAR) Oversight Committee	Member	7/04 – 9/05
University Academic Senate	Senator-Deans' Rep	8/05 – 5/07
Academic Senate Executive Committee	Member	8/06 – 5/07
Presidential Mission Statement Task Force	Member	9/05 – 3/06
University Commercialization Advisory Board	Member	10/05 – 7/09
Cyber Infrastructure Advisory Committee	Member	10/05 – 3/06
Advancement Policy Council	Member	12/05 – 3/09
Effort Reporting for Sponsored Research - Steering Committee	Member	1/06 – 10/08

USTAR Building - Steering Committee	Member	5/06 – 12/11
Disaster Resistant University Advisory Com.	Member	8/06 – 10/08
Internal International Advisory Board	Member	10/06 – 12/08
Asia Center Advisory Board	Member	8/07 – 7/10
Communication, Leadership, Ethics and Research (CLEAR) Advisory Board	Member	9/07 – 6/13
USTAR Bldg. Programming Committee	Member	1/08 – 12/11
Quadrangle Master Planning Committees		
Open Space Committee, Design Committee		
NanoFab Subcommittee		
Dean College of Pharmacy Search Committee	Member	10/08 – 10/09
Mathematics Steering Committee	Member	9/08 – 12/11
Endowment Advisory Committee	Member	12/09 – 7/11
Assoc VP for Enrollment Management Search Committee	Member	12/10 – 7/11
Chief Information Officer Search Committee	Member	1/11 – 5/11
Director Technology Commercialization Office Search Committee	Member	3/11 – 9/11
Senior Vice President Academic Affairs Search Committee	Member	2/12 – 7/13
Operational IT Committee	Member	2012 – 2015
Songdo Steering Committee	Member	2012
U of U Branding Committee	Member	1/12 – 8/12
Budget Principles and Process Working Group	Member	2013 – 2014
Search Committee Chief Business Officer	Member	2013 – 2014
Fundraising Working Group	Member	2013 – 2015
Chair of Search Committee for Dean of Science	Co-Chair	01/13 – 04/14

College Board AP Engineering Committee	Member	10/13 – 10/14
Space Allocation Working Group	Member	2013 – 2014
Office of Global Engagement Council	Member	2014 – 2018
Chief Information Officer Search Committee	Member	7/13 – 12/14
Dean’s Advisory Group to the Provost	Member	10/14 – 10/16
USAID Pakistan Water Advisory Board	Member	3/14 – 12/20
Faculty Data Services Committee	Member	5/15 – 11/15
ARUP Director Search Committee	Member	7/15 – 8/16
Gould Lecture Board	Member	7/15 –
TVC Director Search Committee	Member	6/16 – 1/17
Campus Budget Advisory Committee	Member	1/16 – 6/18
Graduate Writing Committee	Member	1/16 – 12/16
Sustainable Funding Models for Learning Abroad Committee Member and International Student & Scholar Services		1/16 – 12/16
Sr. VP’s Institutional Analysis Committee	Committee Member	7/16 – 6/17
Entrepreneurial Faculty Scholar	Faculty Mentor	10/16 –
President’s Leadership Council (PLC)	Member	10/18 – 5/21
Internal Advisory Board (IAB) for Huntsman Cancer Institute	Member	3/18 – 6/24
RPT Content Committee	Co-Chair	11/18 – 10/19
Rosenblatt Selection Committee	Member	3/19, 3/20
Academic Senate	Member	8/20 – 8/22
Facility Clearance Security Governance Com.	Member	9/24 –
Price Computing and Engineering Bldg. Steering Member & Oversight Committees		11/20 –

Committee Assignments at University of Michigan

(see key below)

<u>Committee</u>	<u>Position</u>	<u>Date</u>
EECS Ad hoc Circuits Review Com.	Member	10/85 – 1/87
SSEL Operations Com.	Member	1/86 – 9/00
EECS Ad hoc Com. on CAD Tools	Chair	3/86 – 12/87
Solid-State Lab Mgr. Search Com.	Member	9/86 – 10/86
EECS Computer Policy Com.	Member	9/86 – 8/91
IEEE Student Chapter Advisor	Advisor	1/87 – 8/90
SSEL Ad hoc Com. on Document Prep.	Chair	2/87 – 4/87
EECS Ad hoc Computing Needs Com.	Member	3/87 – 5/87
EECS Elec. Sci. Eng. Division Executive Com.	Member	9/88 – 8/89
College Honors and Awards Com.	Member	9/88 – 9/90
EECS Elec. Sci. Eng. Division Graduate Com.	Member	9/92 – 8/94
EECS Circuits Advisor	Advisor	9/92 – 8/94
CAEN Executive Committee	Member	10/90 – 8/95
EECS Dept. Executive Committee	Member	9/93 – 8/95 9/97 – 5/03
Solid-State Faculty Search Committee	Member Chair	9/96 – 9/99 9/98 – 9/99
EECS Department Chair Search Committee	Member	11/96 – 9/97
CoE National Advisory Committee	Participant	11/98
DCO Executive Committee	Member	9/97 – 9/98
Circuits Faculty Search Committee	Chair Member	9/97 – 8/98 9/98 – 9/99
Tauber Manufacturing Institute	Board of Directors	9/97 – 9/99

TMI Industrial Co-Director Search Committee	Member	9/98 – 6/99
UM Conflict of Interest Committee	Member	9/95 – 4/01
EECS Administrative Committee	Member	10/97 – 6/01
EECS Honors and Awards Committee	Member	9/97 – 5/03
EECS National Advisory Committee	Participant	3/99
ESE/SSE Curriculum Committee	Member	9/98 – 6/01
CoE Task Force on Reshaping Graduate Engineering Education	Member	9/98 – 6/99
EECS Ad Hoc Committee on Undergraduate Programs	Member	9/99 – 3/00
EECS Futures Committee	Member	3/00 – 11/00
EECS National Advisory Committee	Participant	9/00
CE Undergrad Degree Committee	Member	10/00 – 7/01
EE/Systems Organization Committee	Member	4/01 – 8/01
EECS Administrative Committee	Chair	7/01 – 5/03
ECE Executive Committee	Chair	7/01 – 5/03
CSE Executive Committee	Member	7/01 – 5/03
CoE Chair Advisory Committee	Member	7/01 – 5/03
EECS National Advisory Committee	Organizer	3/02
CoE National Advisory Committee	Participant	4/02
CoE Committee on Interdisciplinary Research	Member	9/02 – 5/03
Medical School Conflict of Interest Board	Member	9/02 – 2/02
CoE International Programs Committee	Member	9/02 – 6/04
Arthur F. Thurnau Professorships	Reviewer	2002 2003

Michigan Society of Fellows	Reviewer	2002
OVPR Review Committee of Conflict of Interest & Commitment Policies	Member	2003
Infrastructure Systems Initiative (ISI) Steering Committee	Member	2003

CoE	College of Engineering
EECS	Electrical Engineering and Computer Science Department
ECE	Electrical and Computer Engineering Division of EECS
CSE	Computer Science and Engineering Division of EECS
ESE	<i>former</i> Electrical Science and Engineering Division of EECS
SSE	<i>former</i> System Science and Engineering Division of EECS
SSEL	Solid-State Electronics Laboratory
CAEN	College of Engineering Computer-Aided Engineering Network
DCO	EECS Departmental Computing Organization
UM	University of Michigan

Administrative Duties at U of Utah

<u>Organization</u>	<u>Duty</u>	<u>Date</u>
CoE	Dean	7/04 – 6/24

Administrative Duties at U of Michigan

<u>Organization</u>	<u>Duty</u>	<u>Date</u>
EECS/CAEN Electronic CAD Application Sector	Director	6/88 – 6/04
EECS Department	Assoc. Chair	10/97 – 6/01
EECS Department	Interim Chair	7/01 – 6/03

Service to Government and Professional Organizations

<u>Type/Organization</u>	<u>Position</u>	<u>Date</u>
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Proposal Reviewer

NIH	Reviewer	
UM Undergraduate Initiatives Grants	Reviewer	
State of Michigan Research Fund Proposals	Reviewer	
UM Office V.P. for Research Grants	Reviewer	
NSF	Reviewer	
Department of Energy	Reviewer	
NIH Site Visit Special Study Section Panel	Member	1998

Journal Reviewer/Editor/Advisory Board

IEEE Transactions on Electron Devices	Reviewer	
Solid-State Electronics	Reviewer	
Analytical Chemistry	Reviewer	
Sensors and Actuators	Reviewer	
IEEE Circuits and Devices	Reviewer	
IEEE Journal of Solid State Circuits	Reviewer	
IEEE Journal of Solid State Circuits	Guest Editor	1995
IEEE Transactions on Reliability	Reviewer	
IEEE Transactions on Very Large Scale Integrated (VLSI) Circuits	Assoc. Editor	1999-2002
IEEE Sensors Journal	Advisory Board	2001-
Proceedings of the IEEE	Guest Editor	2001-2002
American Society of Engineering Education	Reviewer	

Advisory Committees and Activities

	Panel Member	1990
NSF Workshop on Microelec. Sys. Edu. in the 1990s	Member	1990
ASME Emerging Technologies Com.	Panel Member	1993
NSF Workshop on Rapid Prototyping of ICs	Member	1993
ARPA/ONR Thermal Management Round Table	Member	1993 – 2012
MOSIS Advanced Technology Advisory Committee	Panel Member	1996
NSF Workshop on Integration of Edu. & Res. in Microelec. Edu.	Chair	1997 – 2012
NSF MOSIS Advisory Council on Education	Member	1999
Engineering Program Review for BYU ECE Dept.	Member	2000 – 2005
National Advisory Committee for BYU ECE Dept.	Member	2001 – 2004
SRC Undergraduate Engineering Programs Advisory Board	Member	2004 – 2019
Hope College Engineering Advisory Board	Member	2004 – 2019
Utah Technology Council	Member	2008 – 2019
Utah Technology Council Utah Quality TECH Workforce	Member	2006 – 2021
Utah Technology Council Public Policy Committee	Member	2006, 2010, 2014
University of Washington, College of Engineering Visiting Com.	Member	2014
IEEE CS Fellows Evaluation Committee	Member	2012-2013
IEEE Sensors Fellow Committee	Member	2012, 2013
Council On Competitiveness	Member	2014
IEEE Sensor Council Fellow Evaluation Committee	Committee	2011 – 2012
Engineering Deans Council Public Policy Colloquium	Member	2013 – 2015
IEEE Frederick Philips Award Committee	Member	2012 – 2013
IEEE Sensors Council Technical Achievement Award	Member	2013
College Board AP Engineering Committee Member	Member	2014 – 2016
IEEE Robert N. Noyce Medal Selection Committee Member	Chair	2016 – 2018
IEEE Robert N. Noyce Medal Selection Committee Chair	Committee	2017 – 2018
Engineering Deans Council Public Policy Colloquium	Chair	2016 – 2018
IEEE Medals Council	Member	2017 – 2018
Envision Utah Point of the Mountain Education Committee	Member	2017 – 2019
Envision Utah Board of Directors	Member	2020 –
IEEE Sensor Council Fellow Evaluation Committee	Member	2021 – 2022
ASEE Engineering Deans Nominating Committee	Member	2022 – 2024
Morgan State University Engineering Executive Council Idaho	Member	2022 –
National Laboratory Energy & Environment Science & Technology Strategic Advisory Committee		

Program Committees

VLSI Education Conference		1989
Advanced Research in VLSI		1992
27th Hawaii International Conference on System Sciences		1993
GaAs IC Symposium		1993 – 1997
Advanced Research in VLSI		1995
Advanced Research in VLSI Program Chair	Chair	1999
Ninth Great Lakes Symposium on VLSI		1999
Microelectronic Systems Education Conference		1999
Advanced Research in VLSI		1999
DAC 2000 (Chair of Student Design Contest)	Chair	2000
SPIE'S Int'l. Symp. on Microtechnologies for the New Millennium		2003
Microelectronic Systems Education Conference (MSE) 2003		2003
2004 IEEE Intl. SOI Conference		2004
Microelectronic Systems Education Conference		2005
2005 SOI Conference		2005

Executive/Organizing Committees

Symposium on Cellular Bioengineering	Org. Com. Mem.	1987
Instrument Soc. of America, Symp. on Innov. in Meas. Sci.	Session Org.	1988
IEEE/NSF Multichip Module Workshop	Org. Com. Mem.	1991
IEEE Mid-America Symposium on Circ. and Sys.	Org. Com. Mem.	1993
1995 GaAs IC Symposium	Treasurer	1995
1996 GaAs IC Symposium	Publicity Chair	1996
1997 GaAs IC Symposium	Publicity Chair	1997
1997 Conference on Advanced Research in VLSI (at UM)	General Chair	1997
Ninth Great Lakes Symposium on VLSI	Executive Com.	1999
Microelectronic Systems Education Conference 2001	Chair	2001
Public Policy Committee of the ASEE Eng. Deans Council	Org. Com. Mem.	7/11 – 6/12
ASEE Public Policy Colloquium	Member	2012
2014 ASEE Engineering Deans' Institute	Org. Com. Mem.	2013
ASEE Public Policy Colloquium	State Leader	2014
PAC-12 Engineering Deans	Organizer	2016

Consulting and Industry Board Memberships

Consulting has played an important role in keeping Prof. Brown current on VLSI and CAD topics, bringing industrial and government funding to his research group, forming critical relationships to aid in his research, and enriching the courses he has taught (e.g., the 16-bit RISC processor which is used as the baseline design in EECS427 is a proprietary National Semiconductor architecture, used with permission). In addition, he has had the exhilarating experience of helping define the next generation of microprocessors and VLSI CAD tools, and seeing some of his research work in several areas have an impact in commercial products.

Cardinal Industries, Webb City, MO	9/81 – 5/93
Integrated Microsystems, Inc., Ann Arbor, MI	9/86 – 12/86
General Electric Corporate R&D, Schenectady, NY	7/87
Seattle Silicon, Inc., Seattle, WA	10/87 – 8/91
Fleck Controls, Inc., Brookfield, WI	7/90 – 3/94
Cascade Design Automation, Seattle, WA	9/91 – 1/98
DuPont Medical, Newark, DE	3/93 – 5/95
Motorola Semiconductor Prod. Sector, Phoenix, AZ	7/93 – 3/95
Leeds & Northrup, North Wales, PA	8/94
Burns, Doane, Swecker, Mathis, Washington, D.C.	2/95 – 6/95
Idiot Savants, Ann Arbor, MI	5/96 – 4/97
National Semiconductor, Santa Clara, CA	5/97 – 01
Intel Corporation, Santa Clara, CA	7/96
Advanced Micro Devices, Austin, TX	3/97
Giner, Inc., Waltham, MA	1/97 – 7/97
Advanced Sensor Technologies, Inc., Farmington Hills, MI	10/98 – 1/00
Collaboration by Design, Dallas, TX	2/99 – 1/00
Ardesta, LLC	12/00 – 6/04
Maryland Higher Education Commission	8/00 – 5/02

i-sens - Scientific Advisory Board Member*	3/00 – present
Mobius Microsystems Board of Directors*	7/02 – 12/05
Chair of Mobius Advisory Board*	12/05 – 1/10
V-Spring Capital	12/05 – 1/06
e-SENS, Chairman of the Board*	12/10 – present
CoaguSense, Inc., Board Member	10/16 – present
University of Arkansas	5/18
Arkansas Gov. Hutchinson Innovation Council	2/19

Honors and Awards

	<u>Date</u>
Sigma Xi Membership	2025
Utah Academy of Engineering and Science Founding Member	2021
H. E. Thomas Presidential Endowed Deanship	2020
University of Utah Rosenblatt Prize for Excellence	2018
IEEE Life Fellow	2017
National Academy of Inventors Fellow	2016
Utah Governor's Medal for Excellence in Science & Technology	2015
Alumni Achievement Award, Ira A. Fulton College of Engineering and Technology, Brigham Young University	2014
IEEE Fellow Award	2014
Distinguished Alumnus of the Department of Electrical and Computer Engineering, Brigham Young University	2010
Distinguished Young Alumnus, Electrical and Computer Engineering Department, University of Utah	2003
Arthur F. Thurnau Endowed Professorship, University of Michigan	2001
Austin Center for Advanced Studies Fellow, IBM	7/01 - 12/05
Distinguished Faculty Award from Michigan Association of Governing Boards of Universities and Colleges (one of two at University of Michigan)	2000
EECS Department Research Excellence Award, University of Michigan	1995
State of Michigan Teaching Excellence Award (one of 18 in Michigan)	1990
IEEE Student Chapter 1988 Faculty Award, University of Michigan	1988
College of Engineering Teaching Excellence Award, University of Michigan	1987
Member of Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi	

Patents Issued

Richard B. Brown and Noland E. Vogt, "Printer Unit," U.S. Design Patent D270,732, Sept. 27, 1983.

Richard B. Brown, "Integrated Circuit for a Chemical-Selective Sensor with Voltage Output," U.S. Patent 4,743,954, May 10, 1988.

Richard B. Brown and Geun Sig Cha, "Solid State Ion Sensor with Silicone Membrane," U.S. Patent 5,102,526, April 7, 1992.

Richard B. Brown and Geun Sig Cha, "Solid State Ion Sensor with Polyimide Membrane," U.S. Patent 5,417,835, May 23, 1995.

Ajay Chandna and Richard B. Brown, "High Speed Current Mirror Memory Cell Architecture," U.S. Patent 5,490,105, Feb. 6, 1996.

Richard B. Brown, Geun Sig Cha and Howard D. Goldberg, "Batch Deposition of Polymeric Ion Sensor Membranes," U.S. Patent 5,607,566, March 4, 1997.

Hal C. Cantor, Richard B. Brown, Timothy D. Strong, "Microscopic Combination Amperometric and Potentiometric Sensor," U.S. Provisional Patent Serial No.:60/163,471, July 2000.

Timothy D. Strong, Richard B. Brown, Hal C. Cantor, "Batch Fabrication of Electrodes," U.S. Provisional Patent, Serial No.:60/163,654, July 2000.

Richard B. Brown and Steven M. Martin, "Laminated Devices and Methods of Making the Same," U.S. Patent 6,786,708, Sept. 7, 2004.

Robert W. Hower and Richard B. Brown, "Micromachined Device for Receiving and Retaining at Least One Liquid Droplet, Method of Making the Device and Method of Using the Device," US Patent 6,764,652 B2, July 20, 2004. European Patent EP 01989074.8.

Richard B. Brown, Ching-Te K. Chuang, Peter W. Cook, Koushik K. Das, and Rajiv V. Joshi, "Method of Reducing Leakage Current in Sub One Volt SOI Circuits," U.S. Patent 6,952,113, October 4, 2005.

Koushik K. Das and Richard B. Brown, "Low-Leakage Integrated Circuits and Dynamic Logic Circuits," U.S. Patent 6,933,744, Aug. 23, 2005.

Richard B. Brown and Michael S. McCorquodale, "MEMS-Based, Computer Systems, Clock Generation and Oscillator Circuits and LC-Tank Apparatus for Use Therein," U.S. Patent 6,972,635, December 6, 2005.

Richard B. Brown, Gary D. Carpenter, Fadi H. Gebara, "Ultra High Frequency Ring Oscillator with Voltage Controlled Frequency Capabilities," U.S. Patent 7,113,048, September 26, 2006.

Michael S. McCorquodale, Richard B. Brown, Mei Kim Ding, "Linearizing Apparatus and Method," U.S. Patent 7,132,874, November 7, 2006.

Michael S. McCorquodale, Richard B. Brown, "MEMS-Based, Computer Systems, Clock Generation and Oscillator Circuits and LC-Tank Apparatus for Use Therein," U.S. Patent 7,157,984, January 2, 2007.

Steven M. Martin, Roy H. Olsson, III, Richard B. Brown, Robert K. Franklin, "Microsystem for Determining Clotting Time of Blood and Low-Cost, Single-Use Device for Use Therein," U.S. Patent 7,291,310, Nov. 6, 2007.

Robert W. Hower, Richard B. Brown, "Microsensor With a Well Having a Membrane Disposed Therein," U.S. Patent 7,438,851 B2, Oct. 21, 2008.

Henry S. White, Ryan J. White, Richard B. Brown, Hakhyun Nam, Jun Ho Shim, "Nanopore Based Ion-Selective Electrodes," U.S. Patent 8,123,922, Feb. 28, 2012. International Patent WO 2008030582 A2.

Richard B. Brown and Ondrej Novak, "Sensor with a Membrane having Full Circumferential Adhesion," U.S. Patent 10,359,391, July 23, 2019. EP3482195, June 8, 2022. Also patented in China, Canada, and the European Unitary Patent (18 countries) plus Switzerland, Spain, Great Britain and Ireland.

Richard B. Brown and Ondrej Novak, "Microfluidics Chip with Sensor Die Clamping Structures," U.S. Patent 10,464,063 B2, Nov. 5, 2019. Also patented in China, Canada, and the European Unitary Patent (18 countries) plus Switzerland, Spain, Great Britain and Ireland.

Richard B. Brown and Ondrej Novak, "Microfluidic Chip with Chemical Sensor having Back-Side Contacts," U.S. Patent 10,710,068 B2, Jul. 14, 2020. Also patented in India, China, Canada, and the European Unitary Patent (18 countries) plus Switzerland, Spain, Great Britain and Ireland.

Richard B. Brown and Ondrej Novak, "Microfluidics Chip with Sensor Die Clamping Structures" U.S. Patent 11,331,664, May 17, 2022.

Software Developed

Prof. Brown's group's work on GaAs CAD tools resulted in a commercial package that was available from Cascade Design Automation. It included a program for optimizing placement of datapath modules, a phase-checking program for circuits that use two-phase clocking, GaAs DCFL cell generators, delay macromodels, and power estimators.

Professional Memberships

Registered Professional Engineer, State of Utah.

Member of ASEE, IEEE and ACM, as well as the following IEEE Technical Societies: Solid-State Circuits; Electron Devices; Education; Computer; and Circuits and Systems. Life Fellow of IEEE.

Students

Postdoctoral Fellows

<u>Name</u>	<u>Ph.D. Received</u>	<u>Project Topic</u>	<u>Post Doc</u>
Geun Sig Cha	1989	Solid-State Sensor Membranes	1989 - 1991
Segyeong Joo	2006	Novel Chemical Sensors	2006 – 2008

Ph.D. Committees Chaired

<u>Name</u>	<u>Project Topic</u>	<u>Graduation</u>	<u>(Co-)Chair</u>
Koucheng Wu	High-Temperature CMOS	1990	Chair
Jeffrey A. Dykstra	VLSI GaAs DCFL Circuits	1990	Chair
Howard D. Goldberg	Integrated Solid-State Ion Sensors	1993	Chair
Hal Cantor	Amperometric Endocrine Sensors	1994	Co-Chair (BioE)
Muh-Ling Ger	Refractory Metal-Silicide Micromachining	1994	Chair
Ajay Chandna	GaAs DCFL SRAM for Embedded Applications	1994	Chair
Thomas R. Huff	GaAs DCFL Floating-Point Unit	1995	Chair
Michael Upton	Latency- Tolerant GaAs DCFL CPU	1997	Co-Chair
P. Sean Stetson	Low Phase Jitter Clock Generation	1998	Chair
Phiroze Parakh	Design Methodology for Crosstalk in IC Design	1999	Chair
Todd D. Basso	Resource-Limited Superscalar Microprocessors	1999	Chair
Spencer M. Gold	Quantitative Nonlinear Process Scaling	1999	Chair
Claude Gauthier	Current-Mode I/O	1999	Chair
Koushik Das	Low-Power Circuit Design in SOI-CMOS	2003	Chair
Keith Kraver	Low-Voltage Analog Front End	2004	Chair
Michael McCorquodale	All-Silicon Harmonic Clock Generation	2004	Chair
Timothy D. Strong	Solid-State Neural Sensors	2004	Chair
Robert W. Hower	Optical Solid-State Chemical Sensors	2005	Chair
Alan Drake	LC Clock Generation and SOI DTMOS	2005	Chair
Steven Martin	Integrated Heavy Metal Sensors	2005	Chair
Rahul Rao	SOI Circuits to Minimize Gate Leakage	2005	Chair
Jay Sivagnaname	Unipolar Logic in SOI	2005	Chair
Fadi Gebara	Analog SOI Design	2005	Chair
Matthew Guthaus	Clock Tree Synthesis with Process Variability	2006	Chair

Robert Senger	Low-Power Embedded Microprocessor	2007	Chair
Robert Franklin	Electrochemical Brain Probes	2010	Chair
Amlan Ghosh	Process Parameter Variation Mitigation	2010	Chair
Eric Marsman	Embedded Cochlear Processor with DSP	2011	Chair
Spencer Kellis	DSP for Neural Prosthetics	2011	Chair
Ondrej Novak	UWB Transceiver for Biomedical Implants	2014	Chair
F. Bennion Redd	Embedded Microcontroller for Medical Devices	2015	Chair

M.S. Committees Chaired

<u>Name</u>	<u>Project Area</u>	<u>Graduation</u>	<u>(Co-)Chair</u>
Terry C. Huang	Solid-State Ion Sensor	1989	Chair
Tri Nguyen	Molybdenum Micromachining	1989	Co-Chair
Richard S. Raimi	High-Temperature CMOS	1990	Chair
Shailendra A. Save	GaAs Circuit Compiler	1990	Chair
David Johnson	Verilog to Layout CAD Tools	1991	Co-Chair
Phillip J. Barker	GaAs Bus Interface	1993	Chair
Robert G. McVay	GaAs Microprocessor Testing	1993	Chair
Thomas A. Hoy	GaAs Cell Generation	1994	Chair
C. David Kibler	GaAs SRAM Compiler	1994	Chair
David Putti	GaAs Load/Store Unit	1994	Chair
Mark E. Roberts	GaAs Processor Architecture	1994	Chair
Vince Mazzotta	High Perf. Systems	1996	Chair
Michael J. Kelley	Dynamic CGaAs Multiply/Acc. Unit	1997	Chair
John Wei	Low-Noise Mixed Signal Circuits	1999	Chair
Himanshu Sharma	Low-Power Microcontroller	1999	Chair
John Hall	Known-Good Die Testing	1999	Chair
Michael E. Poplawski	Whole Blood Sensor Array	1999	Chair
Jay Cameron	Low-Voltage Analog Design	2000	Chair
Edward Kohler	Instruction Compression for ARM	2000	Chair
Brian Larivee	Low-Voltage Analog Circuits	2002	Chair
Scott Pernia	Low-Voltage ADC	2003	Chair
Yunbum Jung	Cell Library Generation	2003	Chair
Daniel Burke	Electron-Relay Enabled Immunosensor	2003	Chair
Jeff Campbell	Coagulation Sensor	2007	Chair
Nathaniel Gaskin	Harmonic Oscillator-based Sensors	2007	Chair

Ph.D. Committee Member (since 1990)

<u>Name</u>	<u>Project Area</u>	<u>Graduation</u>
<u>Chemistry Department – U of U</u>		
Mark Mendenhall	Glass Nanopore Ion-selective Electrodes	2008
Deric Holden	Soybean Agglutinin Sensor	2012
<u>EECE – IIT Kharagpur</u>		
Dipankar Das	Verification of Multiprocessor Embedded Applications	2009
Sri Ashudeb Dutta	CMOS Low Noise Amplifier For Multi-Standard Receiver	2009
<u>EECS Electrical and Computer Engineering Division – UM</u>		
Jin Ji	Multichannel Intracortical Recording Array	1990
Wei-Tsun Shiau	MOSFET Gate Insulator Reliability at High Temperatures	1990
Steven Cho	Ultra-Sensitive Silicon Pressure-Based Microflow Sensor	1991
Yibing Dong	Instrument for Engine Misfire Detection	1991
Nader Najafi	Smart Sensor with Multi-Element Gas Analyzer	1992
Arnold Hoogerwerf	Three-Dimensional Neural Recording Array	1992
Mark Nardin	Microstimulator with Bi-Directional Telemetry	1996
James Russel Webster	Integrated Capillary Electrophoresis Systems	1999
Uk-Song Kang	Capacitive Humidity Sensor	1999
Andrew Mason	Portable Wireless Multi-Sensor Microsystems for Environmental Monitoring	2000
Pang-Cheng Hsu	Silicon Micromachined Sensors and Actuators	2000
Jeong-Yeop Nahm	a-Si:H TFTs Active-Matrix for Liquid Crystal Display	2000
Joochan Kim	Active Matrix Liquid Crystal Display Technology	2000
Suhwan Kim	True Single-Phase Adiabatic Circuitry for High-Performance, Low-Energy VLSI	2001
Piu Francis Man	Microfluidics for DNA Lab on a Chip	2001
ChuanChe Wang	Contamination-Insensitive Differential Capacitive Pressure Sensors	2001
Yongtaek Hong	Active-Matrix Organic Polymer Light-Emitting Display:	2003
Maysam Ghovanloo	Wireless Microsystem for Neural Stimulating Microprobes	2004
Pedram Mohseni	Bi-directional Wireless Multichannel Microsystems for Biomedical Recording Applications	2005
Gary O'Brien	Angular Rate and Angular Acceleration Sensors	2004
Roy H. Olsson III	1024-Site Multiplexed Recording Array	
Mohamed Abdelmoneum	Micromechanical Wine-Glass Resonators with Semi-Automatic Post Fabrication Trimming	2005

EECS Computer Science and Engineering Division – UM

Robert Masiasz	Exact Layout Minimization of Static CMOS Cells	1991
Yi-Chieh Chang	Load Sharing in Distributed Real-Time Systems	1991
Ayman Kayssi	Timing Macromodels for Digital Circuits	1992
James Dolter	Multi-Mode Router for Real-Time Systems	1993
Khushro Shahookar	Genetic Algorithm for VLSI CAD	1994
Kunle Olukaturu	Technology-Organization Tradeoffs in Computer Architecture	1994
Rich Uhlig	Trap-Driven Memory Simulation	1994
Dan Kaiser	Loop Optimization for Multi-Issue Architectures	1994
Joao Paulo Silva	Algorithms for Satisfiability Problems in Comb. Circuits	1995
Mickael Batek	Test-Driven Transformations in Logic Design	1995
Krishnendu Chakrabarty	Test Response Compaction for Built-In Self Test	1995
Michael Golden	Branch and Load Hazards in Pipelined Microprocessors	1995
Stuart Daniel	Router Architecture for Point-to-Point Networks	1996
Jennifer Rexford	Tailoring Routing Architectures to Performance Requirements	1996
I-Cheng Chen	Branch Prediction via Data Compression	1997
Chih-Chieh Lee	Cache/Branch Prediction Tradeoffs	1997
Bruce Jacob	Operating System Issues in a High Performance Processor	1997
James Dundas	Data Prefetch & Branch Prediction	1998
V. Chandramouli	Timing Models with State Dependency	1998
Hussain Al-Asaad	Verification via Testing-Simulation	1998
Michael Riepe	Leaf Cell Generation	1998
Hakan Yalcin	Timing Analysis	1998
Edward Tom	Improving Cache Performance via Active Management	1999
David Van Campenhout	Design Verification of Microprocessors	1999
Hyungwon Kim	Testing and Synthesis of Systems-On-A-Chip	1999
Jared Stark	Out of order Fetch, Decode, and Issue	2000
Charles Lefurgy	Architecture/Software Interactions in Microprocessors	2000
Brian Davis	Memory Systems Design and DRAM Interfaces	2000
Lea Hwang Lee	Pseudo-Vector Machine For Embedded Applications	2000
Marius Evers	Improving Branch Prediction by Understanding Branch Behavior	2000
Sung-Whan Moon	Quality-of-Service Guarantees in Packet Switched Networks	2001
Gijoon Nam	A Boolean-Based Layout Approach for FPGA Routing	2001
Avinoam Nomik Eden	Branch Prediction - Stretching the Limits	2001
Victor Kravets	Constructive Multi-Level Circuit Synthesis	2001
Hsieu-Hsin Lee	Study of Data Cache Accesses	2001
Matthew A. Postiff	Compiler Optimizations for Register File Use	2001
Hsien-Hsin Sean Lee	Energy and Performance of Data Cache Architectures	2001

Joonhwan Yi	High-Level Function and Delay Testing for Digital Circuits	2002
Alejandro Gonzalez	Resonant-tunneling diodes in digital circuit applications	2002
Fadi Ahmed Aloul	Scalable Algorithms for Boolean Satisfiability	2003
Paul Racunas	Reducing Load Latency	2003
Robert Chappell	Simultaneous Subordinate Microthreading	2004
Rajeev Krishna	Application-specific Processors	2004
Rajiv Ravindran	Hardware/Software Optimizations for Memory Power	2007

Bioengineering -- UM

Steve Freeman	Digital Signal Processing for Ultrasound Images	1998
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Chemistry Department -- UM

Hyoung-Sik Yim	Potentiometric Gas Sensor	1993
Dong Liu	Solid-State Ion/Biosensor Arrays	1994
Ravi Meruva	Gas and Ion Sensing Systems for Biomedical Applications	1997
Bong Oh	Electrochemical Nitric Oxide (NO) Sensor	2003
Hairong Zhang	Redox Enabled Immunosensor	2007

Physics Department -- UM

Nathan Eddy	Analysis of the Top Quark Mass	1998
Eugene Guillian	Top Quark Decay Kinematics	1999

Professional Sketch

The Department of Electrical Engineering and Computer Science at the University of Michigan was a great place for me to grow up academically. The foresight and efforts of those who went before me provided a world-class solid-state laboratory and computing environment which enabled me to be productive in research and effective in teaching. The Department had the perfect environment for me, and it also had needs which I was able to fill. At Michigan I found excellent role models, a stimulating intellectual atmosphere, a spirit of cooperation among the Solid-State Lab faculty, and able and willing collaborators. I received valuable experience as an academic administrator, and was honored to receive research and teaching awards in the department, college and state levels, a distinguished professor designation, and an Arthur F. Thurnau Endowed Professorship.

The years working in industry before the Ph.D. and my industrial sabbaticals provided a perspective which brought relevance to my teaching. I was pleased to hear from many students that the courses they had with me prepared them well for their careers.

I was able to continue my own Ph.D. research, explore new topics, and manage large projects. My research group developed miniature solid-state sensors for applications in monitoring the environment (water chemistry, heavy metals, nanoparticles) and biological fluids (blood electrolytes and gases, pathogens, neurochemicals). We evaluated and contributed to the development of the most advanced semiconductor technologies, designed some of the fastest microprocessors of their time, some of the lowest power microcontrollers, and some of the most highly integrated microsystems. Our semiconductor clocking technology had a significant effect on electronic systems. The solid-state liquid chemical sensors were commercialized in three startup companies, and the all-silicon clock generators were commercialized in a fourth company.

I was able to contribute to VLSI education by developing a much-copied curriculum, and to provide access to chip fabrication for class projects from US universities by raising funds from industry and government as chairman of the NSF MOSIS Advisory Council on Education.

Serving as Dean of Engineering at the University of Utah has been a great opportunity for me. With Engineering Initiative support from the State and the University, private support for facilities, programs and scholarships, and the USTAR initiative, the College of Engineering has been on a steep growth curve in quality and size. Since 2004, the number of Engineering graduates has grown from 484 to 1,379. In 2005, 7% of the U's freshman class selected a major in the College of Engineering; now more than one in five of the freshmen indicate that they are coming to our college. Engineering-related research expenditures have grown from \$30M/yr in 2003 to \$107M/yr. Faculty report more than doubling their peer-reviewed publications over the past decade. The quality of our students, both undergraduate and graduate, continues to rise. The physical facilities in the College have improved dramatically, with the Warnock Engineering Building and Sorenson Molecular Biotechnology Building, and the renovation of the Meldrum Civil Engineering Building, the Warnock Lower Levels, and the Rio Tinto Kennecott Mechanical Engineering Building. In all, we have built or remodeled 1,000,000 ft² of space, and the 250,000 ft² Price Computing and Engineering Building is under construction. The College's social environment has also improved, with the Engineering Alumni Association, Engineering Honors, Engineering Scholars, Engineering Living and Learning Center, Tutoring Centers, junior faculty-dean meetings, faculty research reports to the deans, and more faculty social events. Average course evaluations have steadily improved, and our faculty are advising more than four times as many Ph.D. students. The College of Engineering outreach group has grown the pipeline of students coming into engineering, and our Public Relations team is doing more than ever to publicize the accomplishments of our faculty and students. Since 2006, more than 100 companies have been spun out of the College of Engineering. This progress has required resources, incentives, and broad faculty participation. There is every reason to believe that the momentum will continue.